A LITERATURE REVIEW MULTI-LEVEL INVERTER TOPOLOGIES AND SLIDING MODE CONTROL STRATEGIES

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Abstract

The field of power electronics can be defined to be dedicated to the development of devices that convert one type of power to another. There are four type of power conversions: AC-AC, DC-AC, AC-DC and DC-DC. An inverter circuit is used to convert to DC-AC at desired output voltage and frequency. This conversion can be achieved by transistors, SCRs, MOSFETs, and IGBTs. For low and medium power outputs transistorized inverters are suitable, but for high power outputs SCR’s use is advisable.

One of the biggest problems in power quality aspects is the harmonic contents in the electrical systems. Generally, harmonics are of two types: [51], [65], [70],

1) Voltage harmonics. 2) Current harmonics.

Current harmonics are usually generated by harmonics contained in voltage supply and depend on the type of load such as resistive, capacitive and inductive load. Both harmonics can be generated by either the source or the load side. Harmonics generated by load are caused by nonlinear operation of devices, including power converters, arc-furnaces, gas discharge lighting devices etc. Load harmonics can cause the overheating of the magnetic cores of transformer and motors. On the other hand, source harmonics are mainly generated by power supply with non-sinusoidal voltage waveform. Voltage and current source harmonics imply power losses, electromagnetic interference (EMI) and pulsating torque in AC motor drives.[2], [28],[93]

Multilevel inverters have been attracting in favor of researchers, academia as well as industry in the recent decade for high-power and medium-voltage energy control. In addition, they can synthesize switched waveforms with lower levels of harmonic distortion than an equivalently rated two-level converter. The multilevel concept is used to decrease the harmonic distortion in the output waveform without decreasing the inverter power output. This paper presents the most important topologies like diode-clamped inverter (neutral- point clamped), capacitor-clamped (flying capacitor), and cascaded multilevel with separate dc sources. This paper also presents the most relevant modulation methods developed for this family of converters: multilevel sinusoidal pulse-width modulation, multilevel selective harmonic elimination, and space-vector modulation.[86]

Authors strongly believe that this survey article will be very much useful to the researchers for finding out the relevant references in the field of topologies and modulation strategies of multilevel inverter.

To summarize many multilevel converter topologies proposed during last decade have been reviewed.

Keywords: Diode Clamped Inverter, Capacitor Clamped Inverter, Cascade H-Bridge Inverter, and Sliding Mode Control Technique.
1. Introduction

Numerous industrial applications demand higher power apparatus in recent years. Some medium voltage motor drives and utility applications require medium voltage and megawatt power level. For a medium voltage grid, it is troublesome to connect only one power semiconductor switch directly. As a result, a multilevel power converter structure has been introduced as an alternative solution in high power and medium voltage situations. Subsequently, several multilevel converter topologies have been developed. A multilevel converter not only achieves high power ratings, but also enables the use of renewable energy sources. The term multilevel began with the three-level inverter. The advantages of the multilevel inverter over conventional two-level topology are:[88]

1. The voltage across the switches is only one half of the DC source voltage;
2. The switching frequency can be reduced for the same switching losses;
3. The higher output current harmonics are reduced by the same switching frequency.

The higher output current harmonics are reduced by the same switching frequency. Plentiful multilevel converter topologies have been proposed during the last two decades. Moreover, three different major multilevel converter structures have been reported in the literature: cascaded H-bridges converter with separate dc sources, diode clamped (neutral-clamped), and flying capacitors (capacitor clamped). In summary many multilevel converter topologies have been proposed during last decade. [2], [5],[45]

1.1 Major types of multilevel inverters found in literature are as follows:

A. Diode-clamped Multilevel Inverter (DCMI).
B. Flying-Capacitor Multilevel Inverter (FCMI).
C. Cascaded Multilevel Inverter (CMI).

A. Diode-clamped Multilevel Inverter. [4], [5],[7],[22],[57],[75]

The most commonly used multilevel inverter topology is the diode clamped multilevel inverter, in which the diode is used as a clamping device to clamp the dc bus voltage, so as to achieve steps in the output voltage. Thus, the main concept of this inverter is to use diodes to limit the power device’s voltage stress. The voltage over each capacitor and each switch is \( V_{dc} \). An \( n \) level inverter needs \( (n-1) \) voltage sources, \( 2(n-1) \) switching devices and \( (n-1) \) \( (n-2) \) diodes. By increasing the number of voltage levels the quality of the output voltage is improved and the voltage waveform becomes closer to sinusoidal waveform. Fig.1 shows a five-level diode-clamped inverter in which the dc bus consists of four capacitors, \( C1, C2, C3 \) and \( C4 \), for dc-bus voltage \( V_{dc} \). The voltage across each capacitor is \( V_{dc}/4 \) through clamping diodes.
Fig.1: Circuit diagram of Single phase five level Diode-Clamped Multilevel Inverter.

To synthesize output phase voltage, switching sequence of Single phase five level Diode-Clamped Inverter is given in Table-1

<table>
<thead>
<tr>
<th>Voltage $V_{in}$</th>
<th>Switch State</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{dc}/2$</td>
<td>1 1 1 1 0 0 0 0</td>
</tr>
<tr>
<td>$V_{dc}/4$</td>
<td>0 1 1 1 0 0 0 0</td>
</tr>
<tr>
<td>0</td>
<td>0 0 1 1 1 0 0 0</td>
</tr>
<tr>
<td>$V_{dc}/4$</td>
<td>0 0 0 1 1 1 0 0</td>
</tr>
<tr>
<td>$V_{dc}/2$</td>
<td>0 0 0 0 1 1 1 1</td>
</tr>
</tbody>
</table>

Note- 1- means ON State
0- means OFF State

Table - 1: Switching State of the Five-Level Diode Clamped Inverter

B. Circuit diagram of Single phase five level Flying Capacitor (Capacitor Clamped) Multilevel Inverter: [8],[29],[30],[32],[39]

The structure of this inverter is similar to that of diode-clamped inverter except that, instead of using clamping diodes, the inverter uses capacitors to work as charging device. The flying capacitor involves series connection of capacitor clamped switching cells. This topology has a ladder structure of dc side capacitors, where the voltage on each capacitor differs from that of the next capacitor. The voltage increment between two adjacent capacitor legs gives the size of the voltage steps in the output waveform. Fig.2 shows single phase 5-level configuration of capacitor clamped inverter.
n-level inverter will require a total of \[\frac{(n-1) \times (n-2)}{2}\] clamping capacitors per phase leg in addition to (n-1) voltage sources main dc bus capacitors. The voltage levels and the arrangements of the flying capacitors in the Flying Capacitor Multi-level Inverter structure assures that the voltage stress across each main device is same and equal to \(V_{dc} (n-1)\) for an n-level inverter. The voltage synthesis in a five-level capacitor-clamped converter has more flexibility than a diode-clamped converter. As shown in Fig. 2 the voltage of the five-level phase-leg “a” output with respect to the neutral point ‘n’ (i.e. \(V_{an}\)), can be synthesized with the help of tabulated in Table-2 switching combination.

![Fig. 2.Circuit Diagram of single phase five level Flying Capacitor Multi level Inverter.](image)

To synthesize output phase voltage, switching sequence of five-level flying capacitor inverter is given in Table-2

<table>
<thead>
<tr>
<th>Voltage (V_{an})</th>
<th>Switch State</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>S1</td>
</tr>
<tr>
<td>(V_{dc}/2)</td>
<td>1</td>
</tr>
<tr>
<td>(V_{dc}/4)</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>(V_{dc}/4)</td>
<td>1</td>
</tr>
<tr>
<td>(V_{dc}/2)</td>
<td>0</td>
</tr>
</tbody>
</table>

Note: 1 - means ON State  
       0 - means OFF State

**Table - 2: Switching State of the Five- Level Capacitor Clamped Multilevel Inverter.**

C. Cascaded Multilevel Inverter: [1],[2],[13],[14],[15],[16]

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The concept of this inverter is based on connecting H-bridge inverters in series to get a sinusoidal voltage output. The output voltage is the sum of the voltages that are generated by each cell. The number of output voltage levels are \((2n+1)\), where \(n\) is the number of cells. The switching angles can be chosen in such a way that total harmonics distortion is minimized. One of the advantages of this type of multilevel inverter is that it needs less number of components in comparison to the Diode clamped or the flying capacitor, which results in reduction of weight as well as cost. Fig.3 shows five-level cascaded multilevel inverter.

![Circuit Diagram of singlephase five level Cascaded H-Bridge Multilevel Inverter.](image)

- For an output voltage level \(V_o = V_{dc}/2\), S11, S411 are turned on
- For an output voltage level \(V_o = V_{dc}\), S11, S41 and S12, S42 are turned on
- For an output voltage level \(V_o = 0\), all switches are turn off
- For an output voltage level \(V_o = -V_{dc}\), S21, S31 and S21, S22 are turned on
- For an output voltage level \(V_o = -V_{dc}/2\), S21, S31 are turned on

<table>
<thead>
<tr>
<th>Voltage (V_{ao})</th>
<th>Switching sequence</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{dc})</td>
<td>S11</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>(V_{dc}/2)</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>(-V_{dc}/2)</td>
<td>0</td>
</tr>
<tr>
<td>(-V_{dc})</td>
<td>0</td>
</tr>
</tbody>
</table>

Note- 1 - means ON State, 0 - means OFF State

Table - 3: Switching State of the Five- Level Cascaded H-Bridge Multilevel Inverter.

2. To address the control problem of multilevel inverter, modern control strategies are useful which addresses following issues.
   i) Non-linearity due to the non-linear components in the structure of the inverter,
ii) Stability in steady-state and under line and load variations,

iii) Achieving large-signal stability often calls for reduction of the useful bandwidth. This again affects the inverter performances

iv) Application of these techniques to high-order DC/AC Multilevel inverters may cause a very critical design of the control parameters and a difficult stabilization,

v) Reduction of the costs by reducing the components used in the control prototype, and

vi) Reduction of the electromagnetic interference (EMI) and the space-vector control (SVC).

2.1 Classification of control strategies

The main aim of the modulation strategy of multilevel inverters is to synthesize the output voltage as close as possible to the sinusoidal waveform. Many modulation techniques have been developed for harmonic reduction and switching loss minimization. The modulation methods used in multilevel inverters can be classified according to switching frequency, as shown in Figure 4. Methods that work with high switching frequencies have many commutations for the power semiconductors in one period of the fundamental output voltage. A very popular method in industrial applications is the classic carrier-based sinusoidal PWM (SPWM) that uses the phase-shifting technique to reduce the harmonics in the load voltage. Another interesting alternative is the Space Vector Modulation (SVM) strategy, which has been used in three-level inverters. Methods that work with low switching frequencies generally perform one or two commutations of the power semiconductors during one cycle of the output voltages, generating a staircase waveform. Representatives of this family are the multilevel selective harmonic elimination.

![Fig: 4 Classification of Multilevel modulation methods.](image)

2.2 The classical control methods give good results at an equilibrium point near which the system behavior is approximately linear. Some classical control methods to analyse the stability in linear behavior are listed below:

- Routh-Hurwitz stability criterion,
- Nyquist stability criterion,
- Bode-plot diagram approach,
- The root-locus method, and
- Nichols chart.

2.3 Several tools are available for the analysis of nonlinear systems.

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• The Linearization approximation,
• The Describing function concept,
• The Piecewise-linear approximation,
• The phase plane,
• The Lyapunov’s stability criterion,
• Popov’s method, and
• The Sliding mode control (SMC).[25],[92],[89]

Fig. 5. A block diagram showing some methods used to control DC/AC Multi inverter and the disturbances that have influence on the behavior of the inverter and its stability.

2.4 Sliding Mode Control (SMC) :[86],[89],[92]

It is well known that, classical SMC, which can provide great properties such as insensitivity to parameter variations and external disturbance rejection, is a forceful control scheme for nonlinear systems.

The study of sliding mode control has gained popularity in recent years as a methodology for controlling nonlinear systems with modeling un-certainties and external disturbances. It is known that the crucial and the most important step of SMC design is the construction of the sliding surface s (t) which is expected to respond desired control specifications and performance [96]. The trajectories are enforced to lie on the sliding surfaces.

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Let tracking error in the closed loop system be \( e(t) \)

\[
e(t) = \text{error} = \text{Set point} - \text{Measured output}
\]

\( e(t) = r(t) - y(t) \)

\[
\dot{e}(t) = \dot{r}(t) - \dot{y}(t) \quad (2)
\]

\[
\ddot{e}(t) = \ddot{r}(t) - \ddot{y}(t) \quad (3)
\]

Then a sliding proportional + integral + derivative (PID) surface in the space of error can be defined as \[ ]

\[
s(t) = k_1 e(t) + k_2 \int_0^t e(t) dt + k_3 \frac{de(t)}{dt} \quad (4)
\]

where the coefficients \( k_1, k_2, k_3 \) are strictly positive constants \( k_1, k_2, k_3 \in \mathbb{R}^+ \). If the initial error \( e(0) = 0 \), then the tracking problem can be considered as the error remaining on the sliding surface \( s(t) = 0 \) for all \( t \geq 0 \). If the system trajectory has reached the sliding surface \( s(t) = 0 \), it remains on it while sliding into the origin \( e(t) = 0 \), \( \dot{e}(t) = 0 \) as shown in Fig.6. The purpose of sliding mode control law is to force error \( e(t) \) to approach the sliding surface and then move along the sliding surface to the origin. Therefore it is required that the sliding surface is stable, which means \( \lim_{t \to \infty} e(t) = 0 \); then the error will die out asymptotically. This implies that the system dynamics will track the desired trajectory asymptotically.

The control objective is to determine a control \( u(t) \) such that the closed-loop system will follow the desired trajectory, that is, the tracking error \( e(t) \) should converge to zero. The process of sliding mode control can be divided into two phases, that is, the sliding phase with \( s(t) = 0 \), \( \dot{s}(t) = 0 \), and the reaching phase with \( s(t) \neq 0 \).

Corresponding to two phases, two types of control law can be derived separately. Conceptually, in sliding mode the equivalent control is described when the trajectory is near \( s(t) = 0 \), while the hitting control is determined in the case of \( s(t) \neq 0 \).
The derivative of the sliding surface defined by Eq.(4) can be given as

$$\dot{s}(t) = k_1 \dot{e}(t) + k_2 e(t) + k_3 \ddot{e}(t)$$

(5)

A necessary condition for the output trajectory to remain on the sliding surface $s(t)$ is $\dot{s}(t)=0$

$$k_1 \dot{e}(t) + k_2 e(t) + k_3 \ddot{e}(t) = 0$$

(6)

If the control gains $k_1$, $k_2$, and $k_3$ are properly chosen such that the characteristic polynomial in Eq.(3) is strictly Hurwitz, that is, a polynomial whose roots lie strictly in the open left half of the complex plane, it implies that $\lim_{t \to \infty} e(t)=0$ meaning that the closed-loop system is globally asymptotically stable.

The error $e(t)$ can be defined in terms of physical plant parameters as

$$e(t) = r(t) - y(t)$$

Where $r(t)$ is the command signal and $y(t)$ is the measured output signal. The second derivative of the error $e(t)$ is

$$\ddot{e}(t) = \ddot{r}(t) - \ddot{y}(t)$$

Substituting Eqs (2) and (3) in Equ (6), we get

$$k_1 \dot{e}(t) + k_2 e(t) + k_3 \ddot{e}(t) = 0$$

(7)

The equivalent control $u_{eq}(t)$, is obtained as the solution of the problem $\dot{s}(t) = 0$ which leads to

$$u_{eq}(t) = (k_3 C)^{-1}[k_1 \dot{e}(t) + k_2 e(t) + k_3 \dot{r}(t) + k_2 \ddot{y}(t) + k_3 \dot{y}(t) + k_3 B y(t)]$$

(8)

If the initial output trajectory is not on the sliding surface $s(t)$, or there is a deviation of the
representative point from \( s(t) \) due to parameter variations and/or disturbances, the controller must be designed such that it can drive the output trajectory to the sliding mode \( s(t) = 0 \). The output trajectory, under the condition that it will move toward and reach the sliding surface, is said to be on the reaching phase. For this purpose, the Lyapunov function can be chosen as

\[
V(t) = \frac{1}{2} s^2(t)
\]  

(9)

With \( V(0) = 0 \) and \( V(t) > 0 \) for \( s(t) \neq 0 \). A sufficient condition to guarantee that the trajectory of the error will translate from reaching phase to sliding phase is to select the control strategy, also known as the reaching condition.

\[
\dot{V}(t) = s(t)\dot{s}(t) < 0, \quad s(t) \neq 0
\]  

(10)

To satisfy the reaching condition, the equivalent control \( u_{eq}(t) \) given in Eq. (8) is augmented by a hitting control term \( u_{sw}(t) \), to be determined such that,

\[
u(t) = u_{eq}(t) + u_{sw}(t)
\]  

(11)

The continuous sliding mode control has been selected commonly in SMC problems to avoid chattering of the control force and to achieve the exponential stability.

An approach that complies with the non-linear nature of inverter is represented by the Sliding mode control (SMC), which is derived from the Variable structure control control systems (VSCS) theory. This control method offers several advantages over the classical control methods (Mattavelli 1993), (Rossetto 1994), (Spiazzi 1997), (Forsyth 1998), (Utkin 1999) [1], (Castilla 2000), (Alarcon 2001), such as:

- Stability even for large line and load variations,
- Robustness [87],[91]
- Good dynamic response, and
- Simple to implement.

A variable structure system (VSS) is a control in which the structures of control are changed intentionally during time with respect to the structure control law. The instances at which the changing of the structure occurs are determined by the current state of the system. From this point of view, switch-mode power supplies represent a particular class of the variable structure system (VSS), since their structure is periodically changed by the action of controlled switches and diodes. [1]

The Sliding Mode Control (SMC) for variable structure system (VSS) offers an alternative way to implement a control action, which exploits the inherent variable structure nature of DC/AC multilevel inverters. In practice, the converter switches are driven as a function of the instantaneous values of the state variables in a way that forces the system trajectory to stay on a suitable selected surface in the state space called the sliding surface. The most remarkable feature of the Sliding Mode Control (SMC) is its Robustness property.

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The first step of sliding mode control ‘theory’ originated in the early 1950 which were initiated by S. V. Emel’yanov is VSC – (Variable Structure Control) that means varying system structure for stabilization.

Sliding Mode Control (SMC) theory was founded and advanced in the former Soviet Union as a variable structure control system. Sliding Mode Control (SMC) is a relatively young control concept dating back to the 1960s. SMC theory first appeared outside Russia in the mid-1970s when a book by Itkis (1976) and a survey paper by Utkin (1977), were published in English. The SMC “reachability” condition is based on the Russian mathematician Lyapunov and his theory of stability of nonlinear systems.

The underlying idea of sliding mode control is variable structure control. In variable structure control, the structure of the control input is changed in accordance to the system states. This, in turn would result in dynamics that were not realizable with any constituent structure working alone.

Sliding Mode Control may be defined as follows:

**Sliding mode or motion of the system may be defined as motion of the system along a ‘chosen’ line/plane/surface of the state space with stable dynamics. The control designed with this aim is called as sliding mode control.**

2.5 There are various Sliding Mode Control (SMC) strategies as listed below

2.5.1 Classical Sliding Mode Control.
2.5.2 Discrete Time Sliding Mode Control. [90], [84], [82]
2.5.3 Multirate Sliding Mode Control.

The state feedback control approach gives best performance. However, complete state vector is seldom available for control systems. Further, it is not always desirable to construct state observer, in particular for an uncertain system (generally the case with power system). Hence, one has to resort to output feedback based design. However, complete pole placement cannot be guaranteed using static output feedback. A concept known as multirate output feedback control which is of static output feedback kind and at the same time gives guarantee of closed loop stability has been used by many researchers. This is based on sampling input and output at different rates. However, in these methods robustness is not always possible.

With the extensive development of the sliding mode control theory, its application studies have also progressed radically. This control theory has been successfully applied to various engineering problems. SMC is one of the most popular robust control methods adapted by control engineers.

3. Sliding Mode Control application: [92]

One of the most important features of the sliding mode regime in the VSS is the ability to achieve response that is independent of the system parameters. From this point of view, the DC/AC inverter is particularly suitable for the application of the SMC, because of its controllable state “the system is controllable if every state variable can be affected by an input signal”. The output voltage and its derivative are both continuous and accessible for measurement.

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The control structure consists of two control loops: a linear voltage loop, and a non-linear current loop. The combined loops are the SMC.

According to the proposed design criteria, both control techniques ensure excellent static and dynamic performances, and this, as a result, allows a simple control implementation and a minimum size of the energy transfer capacitor.

Experimental results can be reported and compared with those obtained results with other popular control techniques. The main features of the SMC are:

- Simple to implement,
- Large-signal stability,
- Non-oscillatory response of all state variables,
- Short settling time,
- Robustness.

4. Literature Survey

4.1 Diode clamped multilevel inverter:
Zhiguo Pan, et al. [75], presented a new voltage balancing control for the diode-Clamped multilevel rectifier/inverter system. A complete analysis of the voltage balance theory for a five-level back to- back system is given. The proposed control strategy regulates the dc bus Voltage, balances the capacitors, and decreases the harmonic components of the voltage and current. Grain P. Adam, et al. [57], introduced a new operational mode for diode-clamped multilevel inverters termed quasi two-level operation. Such operation aims to avoid the imbalance problem of the dc-link capacitors for multilevel inverters with more than three levels and reduces the dc-link capacitance without introducing any significant voltage ripple at the dc-link nodes. Baoming Ge, et al. [21], suggested an effective control technique for medium-voltage high-power

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induction motor fed by cascaded neutral-point-clamped inverter. Jeffrey Ewanchuk, et al. [5], addressed a five/nine-level twelve-switch inverter which is described for three-phase high-speed electric machines having a low per-unit leakage reactance. Operational and design details are described for the NPC-CI inverter using a three-limb inductor core, including practical considerations for the inverter construction and operation, [Remove this:480 V/208 V inductor mass comparison between six- and twelve-switch topologies, natural voltage balancing of thecapacitor dc link, and voltage stresses of the free-wheel diodes.] Arash A. Boora, et al. [22], used a new single-inductor multi-output dc/dc converter that can control the dc-link voltage of a single-phase diode-clamped inverter asymmetrically to achieve voltage quality enhancement. The circuit of the presented converter is explained and the main equations are developed. C. Attaianese, et al. [23], proposed a comparative analysis between the classical structure of Neutral Point Clamped (NPC) converter and the emerging active NPC converter. Numerical analyses of losses distribution among power devices for some known carrier based PWM techniques are reported. Jianjing Shi et al. [12], presented a DC bus short circuit protection using the sensed voltage across collector and emitter (i.e., VCE sensing), of all the devices in a leg. This feature is accommodated with the conventional gate drive circuits used in the two level converters. The literature explains the detailed circuit behavior and reasons for resulting in the occurrence of such false VCE fault signals. It also illustrates that such a phenomenon shows dependence on the power factor of the supplied three-phase load. It is shown that the problem can be avoided by blocking out the VCE sense fault signals of the inner devices of the leg. Jin Li, et al. [11], introduced a new nine-level active neutral-point-clamped (9L ANPC) converter which is proposed for the grid connection of large wind turbines (WTs) to improve the waveform quality of the converter output voltage and current. The topology, operating principles, control schemes, and main features, as well as semiconductor device selection of the proposed converter are presented in detail. Robert Stala, et al. [31], focused on investigations of dc-link voltages balance with the use of a passive RLC circuit in a single-phase diode-clamped inverter composed of two three-level legs. This literature also presents mathematical analysis of the PWM modulation method and the inverter operation, and an analytical description of the natural balancing process with contribution of the load current and the balancing circuit current. Jin Li, et al. [11], suggested three-level active neutral-point-clamped zero-current-transition (3L-ANPC ZCT) converter for the sustainable energy power conversion systems. The operation principle and comparison with the 3L-DNPC ZCT are analyzed in detail. Marcelo C. Cavalcanti, et al. [4], addressed new modulation techniques for three-phase transformer less neutral point clamped inverters to eliminate leakage currents in photovoltaic systems without requiring any modification on the multilevel inverter or any additional hardware. Jin Li, et al. [11], used comparison between three level diode neutral-point-clamped zero-current transition (DNPC-3LZCT) inverter and three-level active neutral-point-clamped zero-current-transition (ANPC-3L ZCT) inverter. The two multilevel soft switching topologies are compared with respect to switching energy, volume as well as parasitic inductance influence.

4.2 Cascaded multilevel inverter
Zhongyuan Cheng, et al. [53], suggested a novel switching sequence design for the space-vector modulation of high power multilevel converters. Pablo Lezana, et al. [63], addressed the use of a single-phase reduced cell suitable for cascaded multilevel converters. The results presented confirm that this medium voltage inverter effectively eliminates low frequency input current harmonics at the primary side of the transformer and operates without problems in regenerative mode. H. K. Al-Hadidi, et al. [61], investigated a new configuration for a

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cascade (H-bridge) converter-based dynamic voltage regulator in which the basic cascade converter is supplemented with a shunt thyristor-switched inductor. Yidan Li, et al.[62], presented in this literature a novel dc voltage detection technique, referred to as single multiple-voltage (SMV) detector and it is developed to obtain dc capacitor voltages in the cascaded H-bridge (CHB) multilevel inverter-based static synchronous compensator (STATCOM). Zhong Du, et al. [68], used a cascaded H-bridge multilevel converter as well as the proposed transformers. This literature mainly discusses control of seven-level HCMLI with fundamental frequency switching control and how its modulation index range can be extended using triple harmonic compensation. Zhong Du, et al.[54], focused on a cascaded H-bridge multilevel boost inverter for electric vehicle (EV) and hybrid EV (HEV) applications implemented without the use of inductors. Currently available power inverter systems for HEVs use a dc–dc boost converter to boost the battery voltage for a traditional three-phase inverter. Yu Liu et al.[46], suggested a new feedback control strategy for balancing individual dc capacitor voltages in a three-phase cascade multilevel inverter-based static synchronous compensator. Elena Villanueva, et al. [47], addressed a single-phase cascaded H-bridge converter for a grid-connected photovoltaic (PV) application. The adopted control scheme permits the independent control of each dc-link voltage enabling in this way, the tracking of the maximum power point for each string of PV panels. Farid Khoucha, et al. [20], investigated a hybrid cascaded H-bridge multilevel motor drive direct torque control (DTC) scheme for electric vehicles (EVs) or hybrid EVs. The control method is based on DTC operating principles. Rajesh Gupta, et al. [25], presented in this literature a generalized multiband hysteresis modulation and its characterization for the sliding-mode control of cascaded H-bridge multilevel-inverter (CHBMLI)-controlled systems. A frequency-domain method is proposed for the determination of net hysteresis bandwidth for a given desired maximum switching frequency of the inverter. Domingo A. Ruiz-Caballero, et al. [24], used novel symmetric hybrid multilevel topologies for both; single and three phase medium-voltage high power systems. Gierr Waltrich, et al. [27], proposed a modular three-phase multilevel inverter especially suited for electrical drive applications. The topology is based on power cells connected in cascade using two inverter legs in series. K.Sivakumar, et al. [28], suggested a new five-level inverter topology for open-end winding induction-motor (IM) drive. Farid Khoucha, et al.[26], addressed a comparison study for a cascaded H-bridge multilevel direct torque control (DTC) induction motor drive. In this case, symmetrical and asymmetrical arrangements of five- and seven-level H-bridge inverters are compared in order to find an optimum arrangement with lower switching losses and optimized output voltage quality. Jianjiang Shi, et al. [12], presented in this literature that the solid-state transformer (SST) is one of the key elements in power electronic-based micro grid systems. This literature presents a novel single-phase d–q vector-based common-duty-ratio control method for the multilevel rectifier, and a voltage feed forward and feedback based controller for the modular DAB converter. Makoto Hagiwara, et al. [13], introduced the modular multilevel cascade converter based on double-star chopper-cells, which is intended for grid connection to medium-voltage power systems without using line-frequency transformers. Thus an arm-balancing control to achieve voltage balancing under all the operating conditions is proposed. Hossein Sepahvand, et al. [14], studied the impacts of the connected load to the cascaded H-bridge converter as well as the switching angles on the voltage regulation of the capacitors. This literature proves that voltage regulation is only attainable in a much limited operating conditions that it was originally reported. Javad Ebrahimi, et al. [15], used a new topology of a cascaded multilevel converter. The proposed topology is based www.ijasem.org
on a cascaded connection of single-phase sub multilevel converter units and full-bridge converters. Then the structure of the proposed topology is optimized.

4.3 Flying capacitor multilevel inverter

Byeong-Mun Song, et al. [88], presented in this literature a new soft-switching flying capacitor multilevel inverter that can be generalized and be extended from three levels to any number of levels. Miguel F. Escalante, et al. [85], addressed the requirements imposed by a direct torque control (DTC) strategy on multilevel inverters. A control strategy is proposed in order to fulfill those requirements. Keith A. Corzine, et al.[81], suggested an approach of balancing the capacitors, thus expanding the application fields of FBCS inverters to the family of the flying capacitor multilevel inverters under the condition of choosing a suitable modulation index. Xiaomin Kou, et al.[78], used a unique design for flying capacitor type multilevel inverters with fault-tolerant features. The most attractive point of the proposed design is that it can undertake the single switch fault per phase without sacrificing power converting quality. The capacitor balancing approach under fault conditions are also given. Anshuman Shukla, et al. [76], investigated a method for controlling the FCMLI which ensures that the flying capacitor voltages remain nearly constant using the preferential charging and discharging of these capacitors. A static synchronous compensator (STATCOM) and a static synchronous series compensator (SSSC) based on five-level flying capacitor inverters are proposed. Dae-Wook Kang, et al. [77], presented in this literature a simple carrier symmetric method for the voltage balance off lying capacitors in flying-capacitor multilevel inverters. The carrier-redistribution pulse width modulation (CRPWM) method was reported as a solution for the voltage balance but it has a drawback at the transition of voltage level. Anshuman Shukla, et al. [76], addressed the implementation of a distribution static compensator (DSTATCOM) using an FCMLI. A hysteresis current control technique for controlling the injected current by the FCMLI-based DSTATCOM is also discussed. Robert Stala, et al.[31], focused on investigations of voltage-sharing stabilization with the use of passive RLC circuit in switch-mode flying capacitor dc–dc converters. Also a mathematical analysis of the balancing process in boost and buck–boost converters is presented. M. Hojo, et al. [29], suggested on well-known topology of flying capacitor multilevel converter which has several terminals of different dc voltage and an ac voltage terminal. This literature proposes to utilize the topology as an integrated power conversion module. Pavel Korble, et al.[30], addressed control strategy of flying capacitors multilevel inverters. The main issue is the analysis of the permissible switching states, especially the possibility of the multiple commutations. Z.Oudjbour, et al. [17], used the stabilization of the input DC voltages of five-level flying capacitors (FLFC) voltage source inverters (VSI). A feedback control algorithm of the rectifier is proposed. M.Trabelsi, et al. [8], investigated an experimental photovoltaic (PV) power conditioning system with line connection. The conditioner consists of a flying capacitors multi-cell inverter fed by a dc–dc boost converter. Mostafa Khazraei, et al. [32], presented in this literature two active capacitor voltage balancing schemes for single-phase (H bridge) flying-capacitor multilevel converters. They are based on the circuit equations of flying capacitor converters. These methods are shown to be effective on capacitor voltage regulation in flying-capacitor multilevel converters. Anshuman Shukla, et al. [76], focused on the development of multilevel hysteresis current regulation strategies. Two such strategies have been discussed and some modifications in their control tasks have been proposed to achieve more reliable and improved performance.
5. Summary of the paper.

The following tables give summary of the paper as: (where is table??)

(a). Table 4: Multilevel Inverter Topologies point of view

4.1 From above Table 4, it is concluded that the 27.27% of total literature reviews are based on Diode Clamped Multilevel Inverter, 40.90% of total literature reviews are based on Cascaded H-bridge Multilevel Inverter, 31.83% of total literature reviews are based on Flying Capacitor Multilevel Inverter view points.

4.2 Sliding Mode Control Strategies point of view

These features are ensured in any operating condition, and the transfer capacitor can become small, since decoupling of the input and output stages are not required.

A closed-loop output voltage control method for Zero Current Switching (ZCS) using the Sliding Mode Control (SMC) is studied. It is shown that the dynamic ranges of the output voltage and load resistance are very large, and that the dynamic behavior of the SMC is not affected by input voltage, which shows the robustness of the SMC technique. These features will be verified by computer simulations. The pioneering work in the variable structure control has been done by Vadim Utkin.

6. Conclusion

This paper has addressed a survey of several technical literature concerned with multilevel inverter topologies and sliding mode control techniques. Today, more and more commercial products are based on the multilevel inverter structure, and more and more worldwide research and development of multilevel inverter-related technologies is occurring. This paper cannot cover or reference all the related work, but the fundamental principle of different multilevel inverters has been introduced systematically. Authors strongly believe that this survey article will be very much useful to the researchers for finding out the relevant references as well as the previous work done in the field of multilevel inverter topologies and sliding mode control techniques.

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