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DESIGN A THREE-STAGE COMPARATOR AND ITS MODIFIED VERSION WITH FASTSPEED AND LOW KICKBACK

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ABSTRACT:-

The three-stage comparator and its modified version, which increases speed and lower kickback noise, are shown in this brief. The three-stage comparator in this study has an additional amplification stage in comparison to the conventional two-stage comparators, increasing the voltage gain and speed. The three-stage comparator allows for the use of nMOS input pairs in both the regeneration stage and the amplification stage, further enhancing speed.This is in contrast to the conventional two-stage structure, which employs pMOS input pairs in the regeneration stage. Furthermore, a CMOS input pair is used at the amplification stage of the proposed modified version of the three-stage comparator. By canceling out the nMOS kickback through the pMOS kickback, significantly lowers kickback noise. Additionally, it adds a second signal line during the regeneration step, which further boosts speed. Both the traditional two-stage and the suggested three-stage comparators areimplemented in the same 130-nm CMOS process for straightforward comparison. According to measurements, the redesigned three-stage comparator increases speed by 32% and reduces kickback noise by ten times. This enhancement does not come at the expense of more input noise or referred offset.

Index Terms— Comparator, high speed, low kickback

INTRODUCTION

The comparator serves as a fundamental component in many different kinds of analog-to-digital converters (ADCs) [1],[2]. The comparator speed, kickback noise, input referred noise, and offset are particularly important limitations on the ADC sampling rate and accuracy in highspeed high-resolution SAR ADCs. It is crucial to create a high-performance comparator in this situation. In recent years,various comparator structures have been reported. A classic ~~d~~esign is the Strong-ARM latch in [3] and [4]. No static power, rail-to-rail outputs, and quick comparison due to positive feedback are only a few of its benefits [4]. However, it also has several drawbacks. The modest current source behind the latch is the first factor limiting its regeneration speed. Second, a high power supply voltage is required since there are numerous stacked transistors.

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These difficulties do not exist in two-stage comparators. [5]– [11]. As an illustration, consider Miyahara's two-stage comparator in [9]. (See Fig. 1).

The modest current source is no longer a constraint on its rate of regeneration. This is because its latch input pair M6- M7 has a gate-source voltage of VDD, which is twice as high as the Strongarm latch's VDD/2. Reducing the number of stacked transistors is an additional benefit. The need for the power supply voltage is loosened as a result.

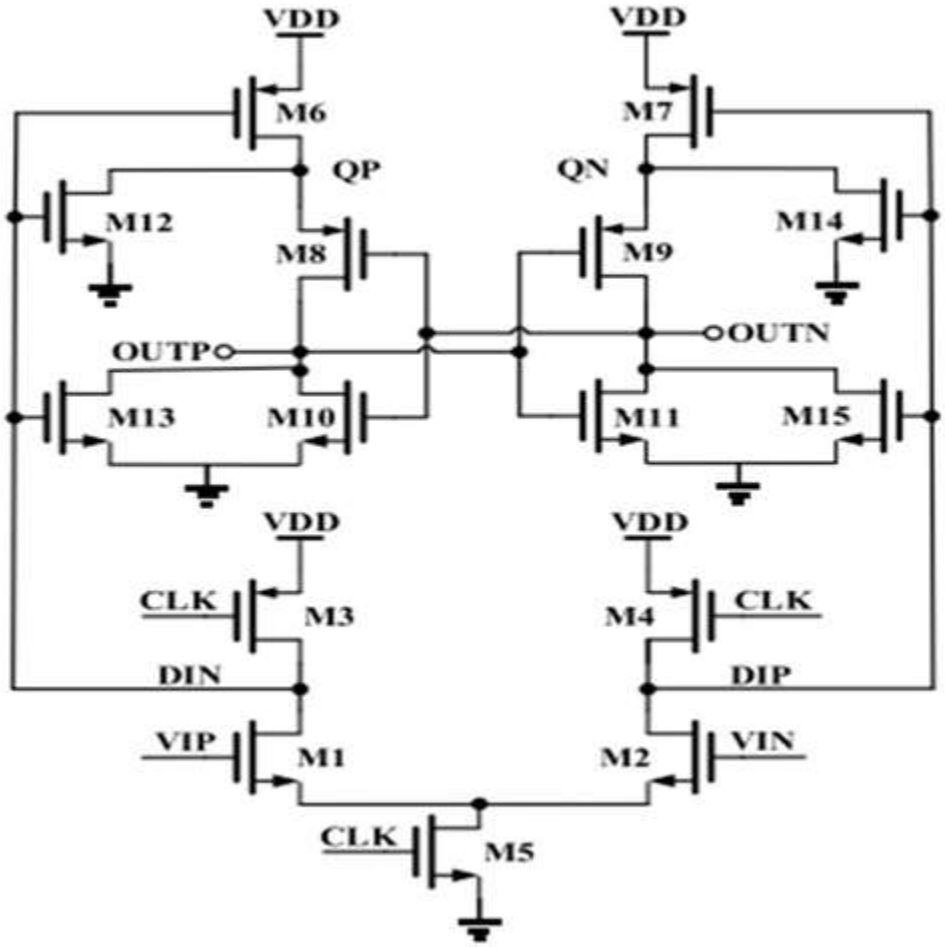

Fig. 1. Miyahara’s two-stage comparator in [9]

Although Miyahara's two-stage comparator speeds things up, there is always room for improvement. The latch input pair M6-7 of this device are pMOS transistors, as seen in Fig. 1, and the regeneration speed is constrained by the low pMOS hole mobility (2–3 times lower than the nMOS electron mobility). Thus, to significantly increase the regeneration speed, our goal is to

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replace the latch input pair with nMOS transistors. The nMOS transistors for the preamplifier input pair must be maintained in the interim.

This brief provides a three-stage comparison to that aim. The nMOS input pairs can be used for both the latch stage and the first-stage preamplifier by including an additional preamplifier stage, which accelerates regeneration. Additionally, these input pairs operate in the saturation area early in the comparison, guaranteeing low input referred noise. Voltage gain is additionally provided by the additional preamplifier stage, which further accelerates regeneration while reducing input referred offset and noise. The three-stage comparator in this study is faster and produces less input referred noise than the previous three-stage comparator [12].

In addition, a modified version of the three-stage comparator is suggested. The first-stage preamplifier's kickback noise is significantly decreased by employing a CMOS input pair. To accelerate regeneration even more and reduce input referred offset and noise, a second path is added in the latch stage. The three-stage comparator in this study is implemented in the same 130-nm process and speeds up by 25% compared to the traditional two-stage comparator. The updated version that is suggested speeds up by 32% and reduces kickback noise by 10 times. This enhancement does not come at theexpense of more input noise or referred offset.

This summary is structured as follows. In Section II, the three-stage comparator is covered. The three-stage comparator's modified form is examined in Section III. The simulated and measured findings aredisplayed in Section IV. The brief isconcluded in Section V.

A. THREE-STAGE COMPARATOR Review of Two-Stage Comparator

The two-stage comparator for the Miyahara is shown in Fig. 1. The reset phase, amplification phase, and regeneration phase are the three stages of operation. The comparator is reset while CLK is at zero (reset phase). The input signal VIP-VIN is amplified and transmitted to the latch stage during the amplification phase (CLK = 1). OUTP and OUTN regenerate to VDD or GND during the regeneration phase. As previously established, the latch stage of such a device is restricted to the pMOS input pair

B. Three-Stage Comparator

The three-stage comparator used in this study is shown in Fig. 2. Each of the three phases is tied to the previous one. The primary distinction between this comparator and Miyahara's comparator is the addition of a second-stage preamplifier. This additional preamplifier serves as an inverter and enables the latch stage to use the nMOS input pair M11–12 in place of the pMOS input pair, resulting in faster operation. Additionally, the additional preamplifier offers voltage gain, enhancing regeneration efficiency andreducing input referred offset and noise.

Although the additional preamplifier aids in speeding up the process, the additional stage itself adds to the delay because the amplified signal must pass through two stages instead of one before reaching the latch stage. It is therefore vital to discuss if the additional delay outweighs

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the value it produces. Its outputs FP and FN fall to GND following the first-stage amplification, as shown in Fig. 2. This results in a huge gate-source voltage that is equal to VDD for the second-stage input pair M8–9.

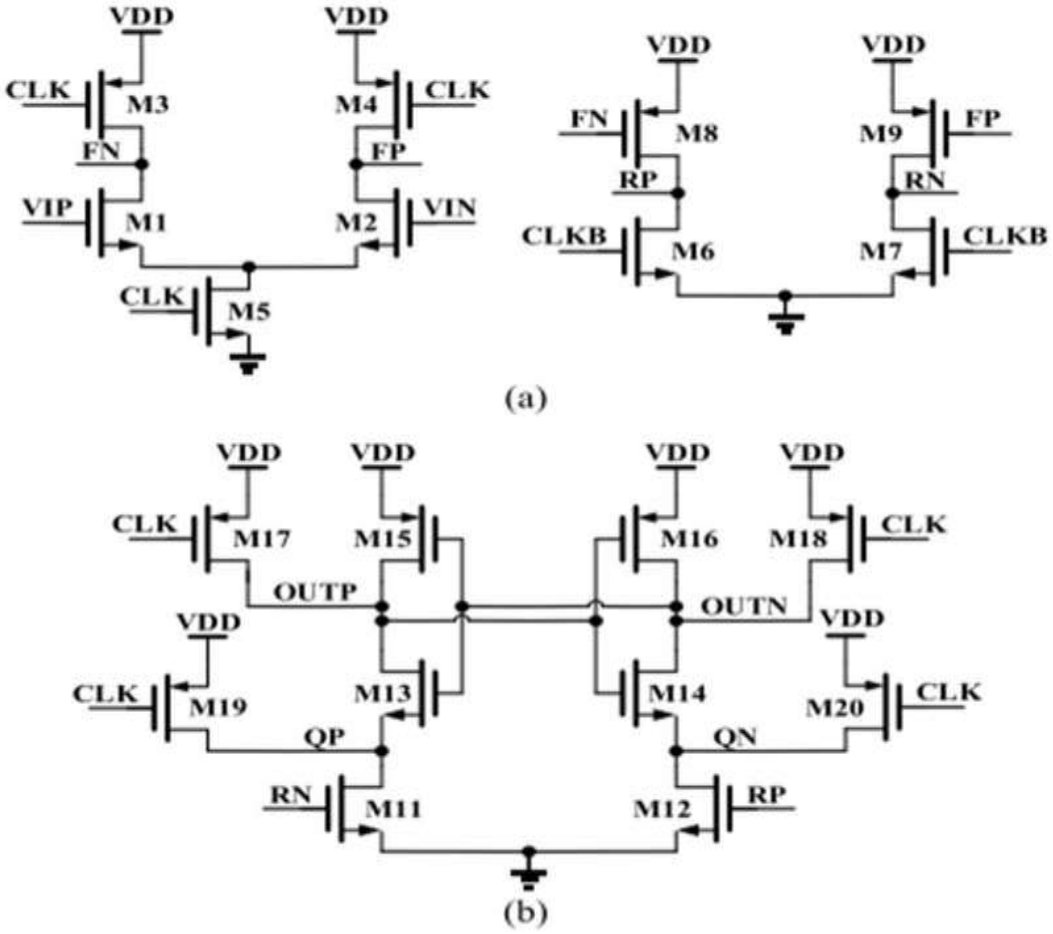

Fig. 2. Three-stage comparator in this work. (a) First two stages (preamplifiers). (b) Third stage (latch stage)

The current on M8-9 is therefore sufficiently strong to quickly drag up RP and RN. As a result, the second stage's additional delay is much smaller (approximately 20 ps in post-layout simulation) than the latch stage's additional delay (about 200 ps in post-layout simulation). This makes sense given that the second stage is a dynamic inverter with minimal delay. Furthermore, the first-stage output load in the three-stage comparator is only M8-9 in Fig. 2 compared to the first-stage output load in Miyahara's comparator (M6-7 and M12-15 in Fig.

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1). The output load is multiplicatively lowered, increasing amplification speed.

The transient simulation comparison of the Miyahara comparator and the three-stage comparator is shown in Fig. 3. As can be seen, the reduced output load causes the three-stage comparator's first-stage outputto settle 60 ps more quickly than the Miyahara's first-stage output.

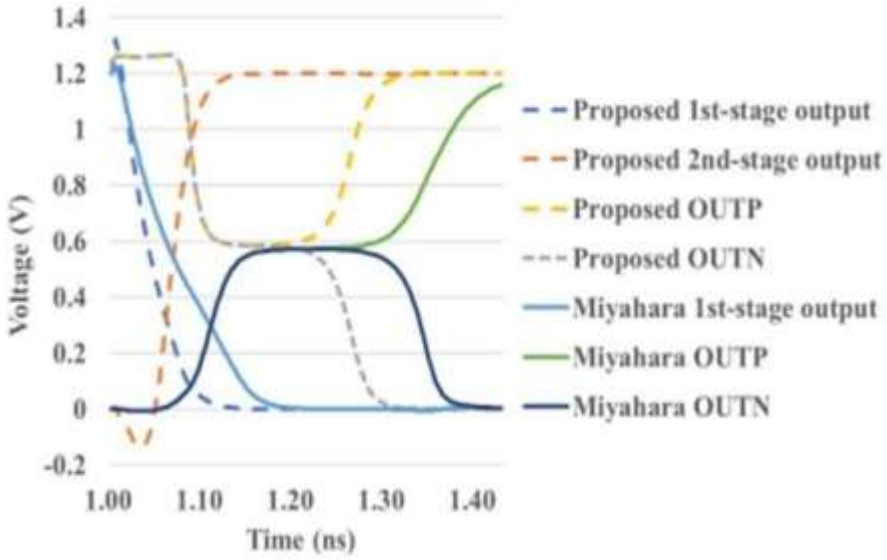

Fig. 3. Transient simulated waveforms of the Miyahara's comparator and the three-stage comparator

The second-stage output of the three-stage comparator settles 40 ps faster than the first-stage output of the Miyahara even after accounting for the second stage's additional delay and 90% settling. Additionally, the nMOS input pair reduces the regeneration time of the latch stage by 76 ps.

The three-stage comparator in this work also has several benefits over the three-stage comparator in [12]. First, rather than being connected to the first-stage output, the gate of M6-7 in Fig. 2 is now connected to CLKB. This reduces the parasitic capacitance at the first-stage output. Second, rather than the second-stage output, the gate of M17-20 is connected to CLK. This lowers the parasitic capacitance at the output of the second stage.

Thirdly, M1-timed 2's cascade nMOS is removed. As a result, the first stage's parasitic capacitance is decreased. More crucially, it assists in ensuring that the M1-2 drain is at VDD at the start of the comparison. This is significant because the input pair's saturation zone aids in lowering input-referred noise.

I. PROPOSED MODIFIED VERSION OF THREE-STAGECOMPARATOR

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A. Circuit Structure

This brief suggests a redesigned three-stage comparator, as depicted in Fig. 4, to lessen kickback noise and further increase speed. The modified version simply differs from the original version in the preceding section by having the extra first two stages of Fig. 4(b) and the extra routes M29-32 in the latch stage of Fig. 4. (c). The additional first two stages use pMOS input pair M11– 12 to remove kickback noise from nMOS input pair M1-2. Additionally, the additional routes M29-32 provide an additional signal to the latching nodes OUTP and OUTN, increasing regeneration speed while further reducing input referred offset and noise.

These additional circuits function as follows. CLK is zero and CLKB is one during the reset phase. In Fig. 4(b), the RP1 and RN1 are reset to GND while the FP1 and FN1 are reset to VDD. In Fig. 4(c), this disables M30 and M32, ensuring that there is no static current in the additional path M29-32. CLK increases to 1 and CLKB decreases to 0 during the amplification phase.

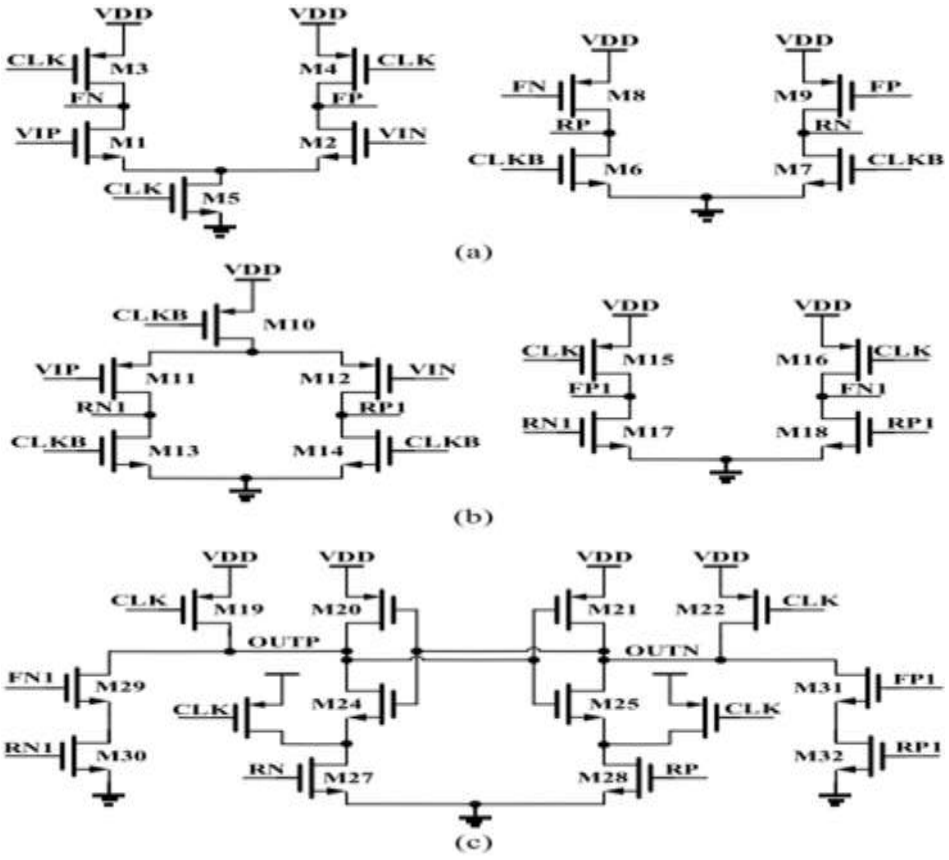

Fig. 4. Proposed modified version of the three-stage comparator. (a) Original first two stages

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(preamplifiers) with nMOS input pair. (b) Extra first two stages (preamplifiers) with pMOS input pair. (c) Third stage (latch stage).

In Fig. 4(b), RP1 and RN1 rise to VDD (R stands for rise). After that, FP1 and FN1 become GND (F stands for fall). Because RP1 and RN1 rise before FP1 and FN1 decrease, the extra routes in Fig. 4(c) are activated for a brief period, and OUTP and OUTN, the latching nodes, are drawn upon to supply a differential current.

This causes a differential voltage to be generated at OUTP and OUTN, which speeds up the regeneration phase subsequently and reduces noise and offset at the comparator input. The extra routes in Fig. 4(c) are turned off once more to stopthe static current after FP1 and FN1 reach GND.

Overall, the updated three-stagecomparator is faster, has less input referee offset and noise, and less kickback noise. It is appropriate for SAR ADCs with high speed and resolution.

TABLE I COMPARATOR DELAY VERSUS INPUT VOLTAGE UNDER DIFFERENT CORNERS (Vcm = 600 mv)

tt corner				
Input	Miyahara	Elzakker	Three-Stage	Modified Version
10 mV	219.93 ps	215.61 ps	170.98 ps	151.85 ps
1 mV	266.37 ps	277.25 ps	213.97 ps	189.52 ps
ff corner				
Input	Miyahara	Elzakker	Three-Stage	Modified Version
10 mV	166.36 ps	168.14 ps	137.21 ps	116.18 ps
1 mV	207.10 ps	226.06 ps	180.47 ps	153.46 ps
ss corner				
Input	Miyahara	Elzakker	Three-Stage	Modified Version
10 mV	306.60 ps	306.18 ps	229.85 ps	193.80 ps
1 mV	373.41 ps	383.27 ps	264.51 ps	225.31 ps

The suggested modified version, for instance, works well with the time-interleaved noise-shaping SAR ADC [13]. Its ADC resolution is constrained by the comparator kickback noise and its ADC speed is constrained by the comparator speed, as mentioned in [13]. Even though Zhuang et al. [13] use channel isolation to lessen the impact of kickback noise, this isolation makes the system more complex. The proposed modified version of the three-stage comparator, however, can address these problems. As will be confirmed later in Section IV, it outperforms other comparators in terms of speed and kickback noise.

B. Design Consideration

According to [14], both the integration time and the input pair transconductance have an

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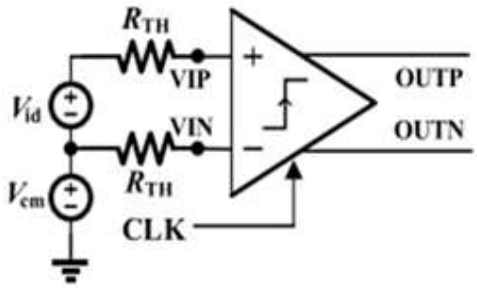
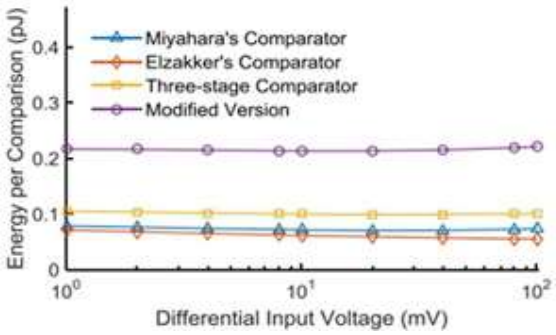
inverse relationship with the comparator input-referred noise. The comparator integration time should be as short as possible due to the use of high-speed, high-resolution ADCs. The input pair transconductance of each stage, including the input pair of each preamplifier and the latch stage, should be increased as much as possible in the meantime to maintain a low input referred noise. To this end, we use large input pair sizes for each stage in this work (W/L is approximately 3 μm/0.13 μm).

II. SIMULATED AND MEASURED RESULTS

A. Post-Layout Simulated Results

This section contrasts this work's three-stage comparators with Miyahara's comparator [9] (Fig 1),Elzakker's comparator [11], and their two-stage comparators. All comparators are post-layout simulated using the same 130-nm process to ensure fair comparison. To compare other specifications all comparators are also built with the same 440 V input-referred noise. The delay is shown in Table I at 90% settling. Input Vcm for common-mode operation is set to 0.6 V. As can be observed, the three-stage comparators consistently have a 15%–25% shorter latency than the two-stage comparators. The updated version's delay is, however, to assess kickback noise [15] as depicted in Fig. 5, where RTH is 4 k, Vid is a differential input of 10 mV, and Vcm is a common-mode input of 600 mV. According to simulation data, the kickback noise for the, 10%–18% is shorter than that of the original version. The circuit four comparators (Miyahara, Elzakker, Three Stage, and Modified Version) are 186.34, 209.61, 223.65, and 19.78 mV, respectively. The improved version has a roughly ten-fold reduction in kickback noise. Fig. 5. Circuit for evaluating the kickback noiseFig. 6. Power consumption versusdifferential input voltage





400 samples are used in a Monte-Carlo simulation to assess the input referred offset. It demonstrates that for the four comparators, the corresponding input referred offset standard

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deviations are 14.04, 13.36, 10.74, and 9.68 mV. The three-stage comparator reduces the offset by 24% and 20%, respectively, when compared to the two-stage comparators (Miyahara and Elzakker), and by 31% and 27%, respectively, for the modified version. The additional preamplifier with additional gain to control the offset is what makes this improvement possible.

The power usage is plotted against the differential input voltage in Figure 6. As can be observed, because of the additional circuits and the higher level of complexity, three-stage comparators use more energy than two-stage comparators.

The three-stage comparators provide significant advantages over the two-stage comparators despite using more power. For instance, even if their power consumption is raised, two-stage comparators cannot operate at a higher pace than three-stage comparators. This is a result of the trade-offbetween speed and power being limited. Larger transistor sizes result from higherpower consumption, which raises parasitic capacitances. This means that even with higher power usage, the speed cannot be significantly increased. The three-stage comparators, in contrast, actually slow down the speed by using more power. The three-stage comparators have this advantage.

Overall, the three-stage comparators' enhanced speed and less kickback are their main selling points. And this does not comeat the expense of an increase in input noise or referred offset.

B. Measured Results

The same 130-nm technology is used for the fabrication of all four comparators. The die images of the three-stage comparators are displayed in Fig. 7. Because there is a limited amount of room in this brief, we do not display the die images of the two-stage comparators.

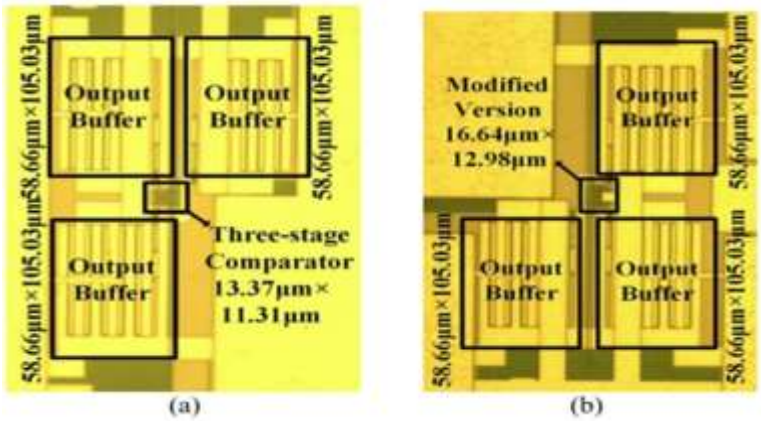

Fig. 7. Die photographs of (a) the three-stage comparator and (b) a modified version of the three-stage comparator

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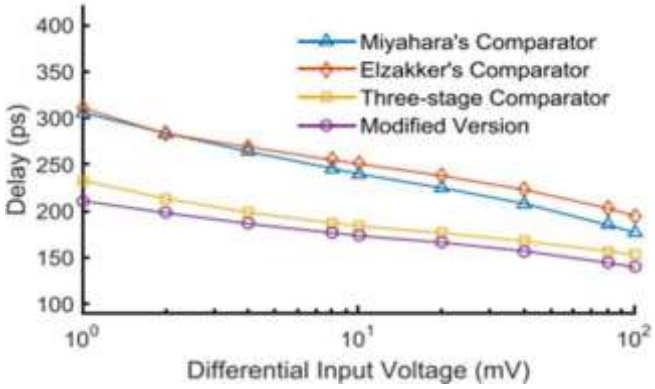

Fig. 8. Measured delay versus differentialinput voltage.

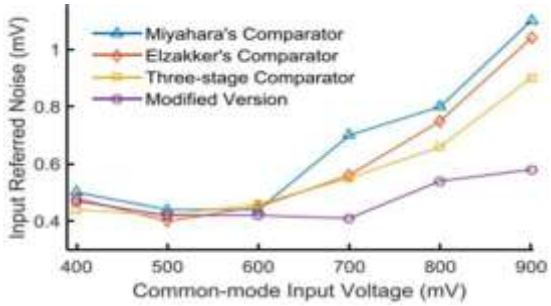

Fig. 9. Measured input referred noise versuscommon-mode input voltage.

Figure 8 depicts the calculated delay. 22chips are measured for each comparator, and a mean value is computed. As can be observed, the three-stage comparator decreases the delay by approximately 25%, while the updated version reduces the delay by approximately 32% when compared to the two-stage comparators. This corresponds to the results of the post-layout simulation. The input referred noise is plotted against the common-mode input voltage Vcm in Figure 9. The input-related noise is intended to be 0.44 mV at 600 mV Vcm. However, when Vcm > 600 mV, the measured input referred noise increases with Vcm. Due to their higher voltage gain, three-stage comparators also have lower input referred noise than two-stage comparators.

TABLE II COMPARISON WITH STATE-OF-THE-ART WORKS

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	[2]*	[5]	[6]	Miyahara*	Elzakker*	Three-stage*	Modified Version*
Technology (nm)	65	180	180	130			
Supply Voltage (V)	1.2	1.2	1.8	1.2			
Area (μm^2)	125	392	490	79	117	151	216
Low Kickback Noise	No	No	No	No	No	No	Yes
Input Referred Offset (mV)	—	7.8	2	15	17	13	11
Energy per comparison (pJ)	0.034	0.658	0.40	0.109	0.111	0.137	0.215
Input Referred Noise (mV)	0.4	—	—	0.44	0.45	0.46	0.42
Delay	1240 ps @ V_{cm}=0.6 V, V_{id}=1 mV	550 ps @ V_{cm}=0.6 V, V_{id}=1 mV	301 ps @ V_{cm}=0.9 V, V_{id}=1 mV	306 ps @ V_{cm}=0.6 V, V_{id}=1 mV	311 ps @ V_{cm}=0.6 V, V_{id}=1 mV	233 ps @ V_{cm}=0.6 V, V_{id}=1 mV	211 ps @ V_{cm}=0.6 V, V_{id}=1 mV

* Measured results.

This work is contrasted with the most recent works in Table II. The three-stage comparator and its modified variant have the shortest latency, as can be observed. The slightest kickback noise is also present in the modified version. Despite the more complex circuit, the power consumption and area are still less than [5], [6].

CONCLUSION

The three-stage comparator and its modified version, which have the benefits of quick speed, little kickback noise, and little input referred offset and noise, are shown in this brief. The high-speed, high-resolution SAR ADCs are well suited for these comparators. Finally, quantified outcomes confirm the potency of these comparators.

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