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FET BASED SINE WAVE CONTROLLED MULTI LEVEL INVERTER WITH REDUCED THD

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***Abstract*—**

The use of solar power plants for electricity generation is incr easing day by day in order to reduce the environmental impac t. The generated DC power needs to be converted to AC powe r to power AC loads or to connect to the grid without interferi ng with the operation of the grid. Multi-level inverters are a good choice because the output voltage of the multilevel inverter is a step waveform close to a sine wave, which provides fewer harmonics. As the number of levels incr eases, harmonic distortion decreases, but at the same time, the number of required switching points and DC voltage sources increases, thus increasing the complexity of system design and control. The multi-level inverter proposed in this paper can provide 15-level output power for renewable energy applications such as solar photovoltaics using only 7 switches. Complexity and cont rol are reduced because fewer keys are used.

Keywords—Multilevel inverter; 15 level MLI; reduced number of switches; total harmonic distortion.

Abbreviations: *MLI, Multievel Inverter; EMI, Electro Magnetic Interference; PV, Photo Voltaic; NPC, neutral point clamped; PWM, Pulse Width Modulation; THD, total Harmonic Distortion.*

I. INTRODUCTION

Power generation using renewable energy resources is increasing rapidly due to the fast depleting fossil fuel and their impact on the environment. When multiple renewable generation units are interconnected and integrated with the grid, proper synchronization is an important requirement. To connect to the grid an AC is required which is obtained by connecting an inverter in case of solar PV system, as the generation is DC. If the output of the inverter contains harmonics the power injected in the grid pollutes the power system. Thus a proper design of inverter, with reduced harmonic distortion, is a mandate.

In recent years, multilevel inverters have gained more scope as multilevel inverters are able to give out their high operating capability, low switching losses, and higher efficiency with lower output Electromagnetic Interference (EMI). The term 'Multilevel inverter' was first introduced by Nabae et al in the year 1981 with the first concept of the Three-level Multilevel Inverter [1]. Multilevel inverter is gaining its prominence because of its ability to meet the increasing demand of high power rated applications and also the power quality associated with its reduced total harmonic distortion. Multilevel inverters have gained a number of their applications such as UPS, power grid, solar inverter, induction heating and industrial applications with highly powered instruments. Multilevel inverters are nearly able to produce a sinusoidal output-voltage waveform using fundamental frequency switching scheme. A sine wave output is more desirable since many electrical products will be engineered to work at their best with input as sine wave AC power source. In multilevel inverters, multiple voltage sources are added to obtain a stepped waveform. As the number of steps are increased, the waveform looks more close to a sinusoid, thus reducing harmonic content.

II. MULTILEVEL INVERTER TOPOLOGIES

Multilevel Inverters [MLI] are the ones which can give out a stepwise output waveform with the use of power electronic switches, power diodes and some DC voltage source which might be a series/parallel connected PV cells, a renewable source or a battery. Multilevel inverters not only produce low harmonic distortion but also decrease the dv/dt stresses on the equipment [2]. In turn the Electromagnetic compatibility can also be reduced.

Three different types of topologies are available in MLIs. They are diode clamped, Flying Capacitor and Cascaded Multilevel Inverters [3]. In diode clamped MLI, a diode transfers a limited amount of voltage, thereby reducing the stress on other electrical devices [4]. The maximum output voltage is half of the input DC voltage. The diode clamped multilevel inverter was also called the neutral point clamped (NPC) inverter. Cascaded multilevel inverter topology is based on the series connection of each sub cell of the multilevel inverter. Flying capacitor was first introduced by Meynard. This topology has reduncies in inner voltage levels; in other words, two or more valid switch combinations can produce the desired output voltage waveform [5]. Cascaded H Bridge MLIs can be either symmetrical or asymmetrical type. In symmetrical cascaded H-Bridge all the voltage sources used are of same magnitude while in asymmetrical the voltage sources used have unequal magnitudes. Advantages of asymmetrical is that a higher number of levels can be obtained with reduced number of voltage sources. Few researchers have proposed solar based MLI in different literatures [6-8].

III. PROPOSED MULTILEVEL INVERTER

In this paper a hybrid technology is proposed where higher numbers of levels are obtained with reduced number of switches and lesser no. of DC voltage sources. In cascaded MLI using 8 switches we can obtain 7 levels, 12 switches are required for 9 levels and so on. The proposed topology uses only 7 Mosfet switches and three DC voltage

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Sources to obtain 15 levels. In comparison with the conventional 15-level Inverter reduced number of switches used in this topology effectively reduces the switching losses and most importantly the circuit complexity. The DC voltage source magnitude is designed with binary forms of voltage such as V, 2V, and 4V respectively. The designed topology gives out 15-level output voltages; they are 7V, 6V, 5V, 4V, 3V, 2V, V, 0, -V, -2V, -3V, -4V, -5V, -6V, -7V respectively. Depending on the output voltage requirement, V can be chosen appropriately. For example to obtain peak amplitude of 21 volt, the voltage sources required are 3 volt, 6 volt and 12 volt.

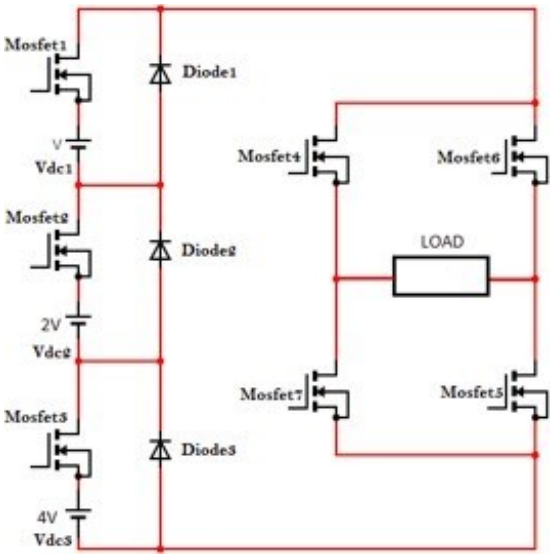
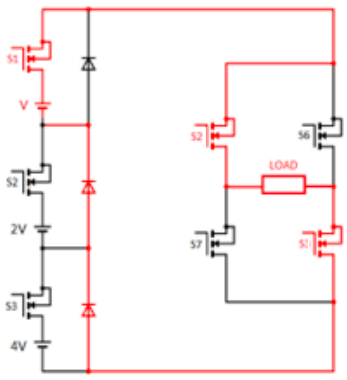


Figure 1: Circuit Diagram of the proposed 15 level MLI

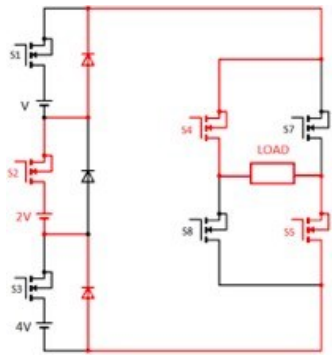
The proposed fifteen level inverter, shown in figure 1, is a combination of three series connected switches with the DC sources with each switch combination having a diode connected in parallel with them.

Table 1: Switching table of the MLI

Vdc	S1	S2	S3	S4	S5	S6	S7
0	0	0	0	1	0	1	0
V	1	0	0	1	1	0	0
2V	0	1	0	1	1	0	0
3V	1	1	0	1	1	0	0
4V	0	0	1	1	1	0	0
5V	1	0	1	1	1	0	0
6V	0	1	1	1	1	0	0
7V	1	1	1	1	1	0	0
-V	1	0	0	0	0	1	1
-2V	0	1	0	0	0	1	1
-3V	1	1	0	0	0	1	1
-4V	0	0	1	0	0	1	1
-5V	1	0	1	0	0	1	1
-6V	0	1	1	0	0	1	1
-7V	1	1	1	0	0	1	1



a. Mode 1 operation [output voltage V]



b. Mode 2 operation [output voltage 2V]

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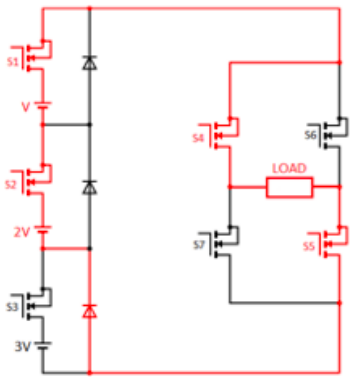
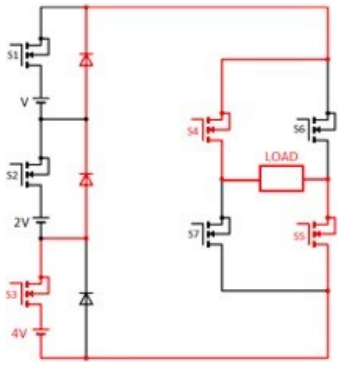
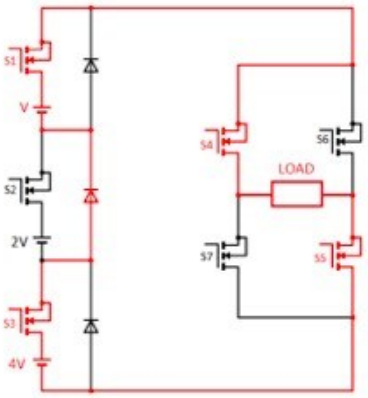


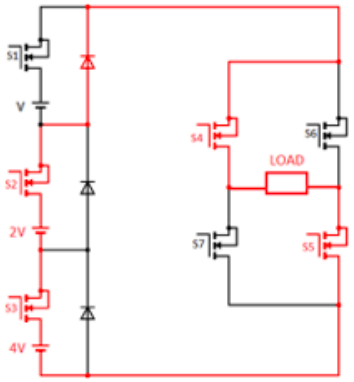
c. Mode 3 operation [output voltage 3V]



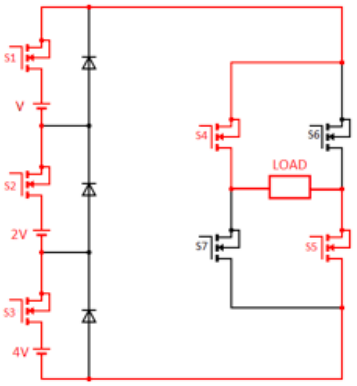
d. Mode 4 operation [output voltage 4V]



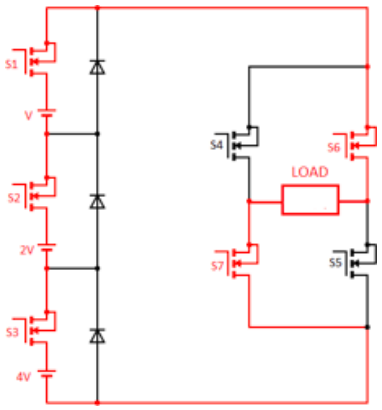
e. Mode 5 operation [output voltage 5V]



f. Mode 6 operation [output voltage 6V]



g. **Mode 7operation [output voltage 7V]**



h. Mode 15 operation [output voltage -7V]

Figure 2: Current flow during different Modes of Operation of Proposed MLI

Diodes not only reduces the stress on the switch but also provides a path for the current flow when the switch is turned off. There is a cascaded H bridge combination that is connected with series connected switches. The pulses to the cascaded cell are given directly through the pulse generator and the pulses to the Mosfet are given as input pulses from the output of the PWM generation circuit.

A. Switching sequence and mode of operation for proposed 15 level inverter

The MLI uses 7 switches to obtain 15 levels. Switches S4, S5, s6 and S7 creates an H-bridge, while S1, S2 and S3 are the series connected switches with the DC sources. Switching table of the inverter is depicted in table 1. For zero volt output from the H bridge either S4 and S6 or S5 and S7

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should be turned on. For positive voltage S4 and S5 should be turned on and to obtain negative voltage S6 and S7 needs to be turned on.

To obtain zero volt, all the series connected switches should be turned off. For 1V, S1 is turned on; for 2V, S2 is turned on; for 3V, S1 and S2 are turned on; for 4V, S3 is turned on; For 5 V, S1 and S3 are turned on; for 6V, S2 and S3 are turned on; for 7V, all S1, S2 and S3 are turned on. The switch position for negative voltages remains the same for S1, S2 and S3 and but in the H-bridge switches instead of S4 and S6, S5 and S7 are to be turned on. Figure 2 shows the mode of operation in different stages and the switches that conduct during the respective mode.

IV. RESULTS AND DISCUSSION

Figure 3 shows the overall block diagram of the system. As the asymmetrical MLI requires sources of different levels of voltages, as per requirement of the output voltage, a number of solar PV can be connected in series. Since the output voltage of solar PV depends on the solar radiation, a buck boost converter can be used to obtain a constant output voltage. To obtain 15 levels using the proposed topology three different levels of voltages are required.

Accordingly three buck boost converters are required. The system is simulated in MATLAB SIMULINK environment. The simulink model of the buck boost converter is shown in figure 4, where the actual voltage generated by the solar PV is converted to a constant voltage matching the reference voltage. Figure 6 shows the voltage waveform with a reference voltage of 12 V. The simulink model of 15 level inverter is presented in figure 5 and the output voltage waveform is shown in figure 7. Depending on the output voltage requirement the magnitude of the DC voltage sources can be chosen.

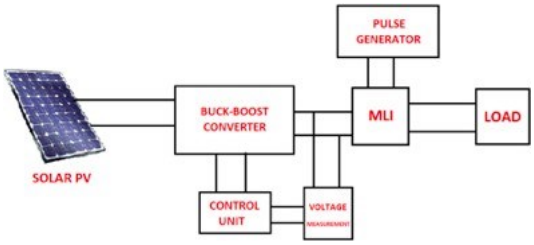

Figure 3: Block Diagram of Overall System

The simulation is conducted with 48 V, 96 V, 192 V DC sources to obtain 325 V peak amplitude which gives 230 V RMS output.

Figure 8 shows the FFT analysis where we can see the Total Harmonic Distortion is 4.7% which is within the acceptable limit as per IEEE 519 standard.

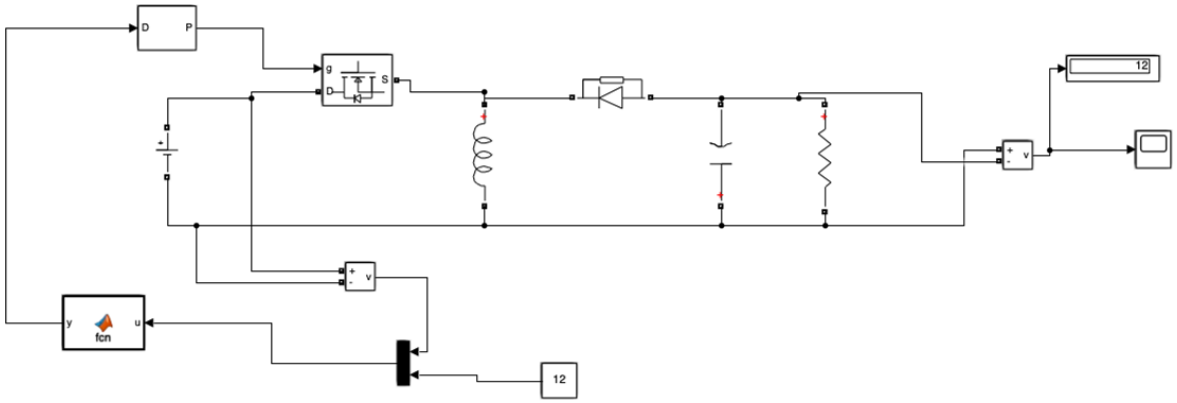

Figure 4: Simulink model of BuckBoost converter

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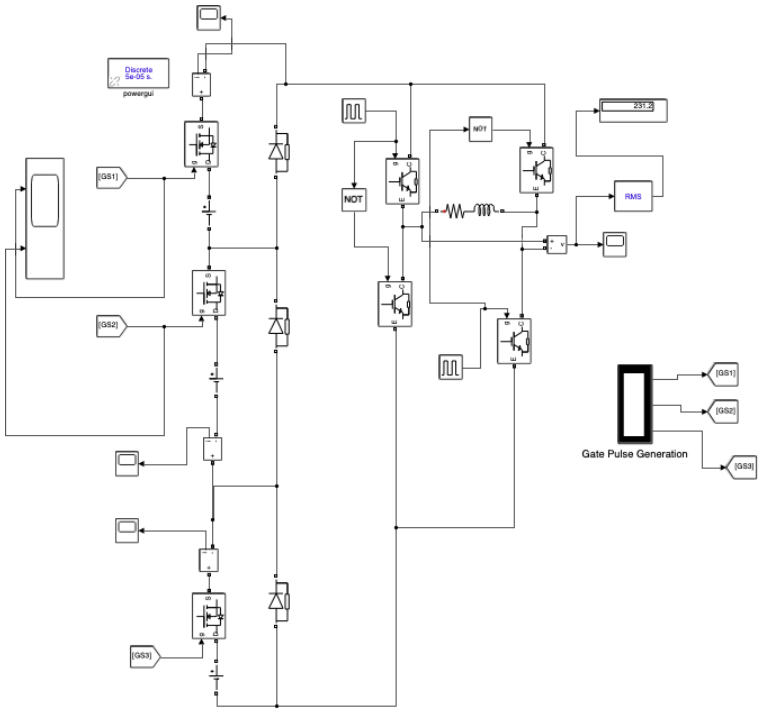

Figure 5: Simulink Model of 15 level Inverter

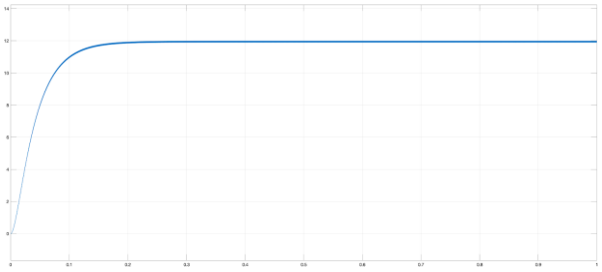

Figure 6: Output waveform of Buck-Boost Converter

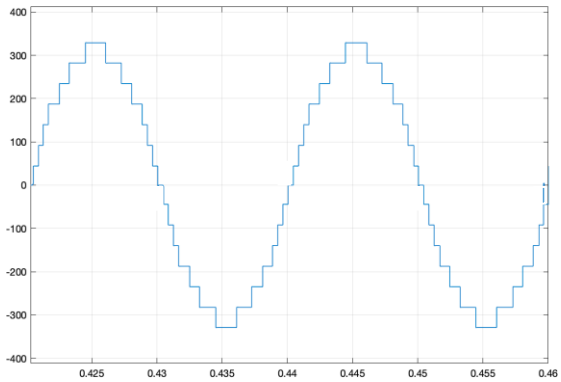

Figure 7: Output voltage Waveform of MLI

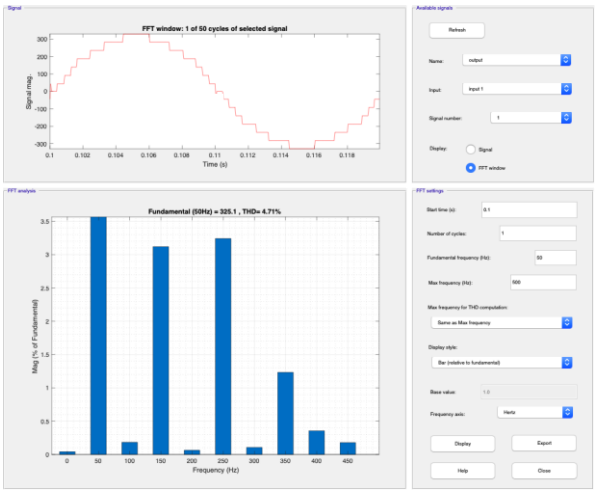

Figure 8: FFT analysis of 15 level inverter's output voltage

V. CONCLUSION

A multilevel inverter with 15 levels is proposed with a reduced number of switching devices. Only 7 switches are used in the proposed system, while 24 switches are required for normal cascaded MLI with 15 levels. Asymmetrical configuration helps in obtaining higher levels with less number of voltage sources. The THD in the output voltage of this 15 level MLI could be brought to 4.71% which is within the acceptable limit.

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VI. FUTURE SCOPE

The proposed multilevel inverter can be used as a drive for solar powered applications. A closed loop control can be developed using intelligent algorithms to optimize the switching angle. The hardware implementation of the proposed work gains more importance for its future scope. Also, the designing and implementation of further levels may reduce the THD to a more lesser values and thereby decreasing and overcoming all the existing problems of the present agenda.

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