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Design and implementation of low power high speed level shifter using CMOS Technology

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ABSTRACT

Modern life isn't possible without tiny, lightweight, and power-efficient devices like smart phones, tablets, media players, and more. One major challenge with emerging technologies is the scalability of voltages. To rescue the day, voltage level shifters are used to feed the circuit with various voltages. Here is a Level up Shifter that can move quickly while using very little power. A dynamic power of $2.0730e-09$, a static power of $1.417e-05$, and an average power of $2.055e-07$ characterize the proposed LS, which is 11 transistors wide. The proposed LS have further advantages when considering overall performance. A level shifter is often located on a SIM, audio, SD, UART, or CF card. With only one supply level shifter, we were able to cut power usage by 45% and delay by 50%. This improves the system's overall performance by making it simpler and cheaper. All of the circuits were simulated using Mentor Tanner 16nmTechnology.

I.INTRODUCTION

Devices like multimedia players, tablets, and smart phones that are small and power efficient are essential in today's environment. As technology advances, a major challenge is the scaling of voltages. In such a case, voltage level shifters are useful for regulating the voltage in the circuit. [1]. Power consumption is a critical factor that affects circuits. Various forms of power consumption exist: (1) Constant power loss; (2) Variable power loss around time. i) Static charge loss: that occurs when a MOSFET's PN junction diode is utilized in reverse, causing current to leak out. ii) Power loss due to dynamic processes, such as charging and discharging the load capacitors. Voltage scaling affects the whole

output voltage swing, leakage currents, and voltage noise margins. The voltage may be adjusted. There will have an effect on micro level technology. Raising a voltage from a lower one is what a level up shifter circuit is all about. System-of-circuits (SOC) design makes use of several voltages to power the many circuits assembled on a single board. If a single block needs many voltages, a level shifter is a lifesaver. Level shifters are important building elements that allow the circuit's inner core to communicate with the IO blocks. A single voltage level shifter allows you to alter the output voltage without requiring additional connection pins.

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II.LITERATURE SURVEY

Our innovative dense wavelength-division multiplexed systems (DWDM) design allows laser transmitters to operate without thermoelectric cooling. This is accomplished by using orthogonal connections between surrounding channels and overlapping arrayed waveguide grating filter profiles. When compared to a traditional DWDM system, this method might reduce power consumption by 68%. To alleviate the burden on existing networks caused by an ever-increasing user base, specifications like as the 40 and 100 Gb/s IEEE 802.3ba have been developed, and publications including results of proof-of-principle experiments using alternating NRZ and Manchester (CAP-2Q) modulation have been made public. It is crucial to meet future requirements in an efficient and cost-effective manner. Data centers are expected to surpass the aviation industry in carbon emissions in 2020 [3], making energy consumption and related operating expenses of utmost importance. An estimated 2-2.5 percent of the world's electricity demand is already attributable to the networking industry [4]. For short-haul data communication lines, wireless service providers are looking to DWDM [5] as a possible solution to meet expected demand. Direct wavelength division multiplexing (DWDM) is a performance-enhancing technique, but it is expensive due to the components required, which need careful control to avoid channel crosstalk and have exact spectral tolerances. Consequently, Coarse WDM has recently become rather popular. Thermoelectric cooling (TEC) modules & wavelength lockers are crucial parts of DWDM for maintaining a consistent wavelength for the transmitter lasers. Failure to do this will cause the wavelength channels to wander due to the thermoelectric effect at a rate of about $0.1 \text{ nm}/^\circ\text{C}$ [6]. The common belief is that the little temperature

difference across the device will cause the wavelength channels of integrated sources to drift together. But there are instances where the channels could go in the same direction, so it's not always the case. If a supervisory/control system does not need a TEC, then considerable power savings may be achieved. Additionally, weak wavelength stability is unnecessary, allowing for the use of cheaper lasers that often fail stability tests. In order for DWDM systems to operate without heat management, many approaches have been devised. But people aren't using this configuration just now. Recognizing it as it transitions between AWG pass bands as a function of temperature becomes possible if each receiving channel has an overlapping profile, since adjacent channels overlap with little insertion loss. Tolerable penalty levels are encountered by DWDM channels even in the most challenging conditions. So, if traditional DWDM systems have failed to address the needs of low-cost data communications, this technology may be worth a try. Following this format will guide the remainder of the article.

III.EXISTING METHOD

This figure depicts LS that uses Current Mirror as its foundation. 1 The input logic 0 causes the circuit operations to be the same as i). M2 will also not be operational, joining M1 and M6 in their non-operational states. Now that node N1 has been charged, the first logic node may proceed. Now we will switch off M4 and discharge node N2 to logic 0. Logic 1 will now be applied to node N3, and M5 will be turned on. So, the output node will go to logic high when M3 & M8 are turned off with the use of M7. Assuming an input signal of logic 1, both M1 and M2 become inactive, and node N1 charges to logic 0, we proceed with an M4. The scenario involves sending Logic 1 to Node N2 and disconnecting Node M5. The logic level for node N3 will be 0, while for node

M6 it will be 1. When M8 is turned on, the output node out will be set to logic zero.

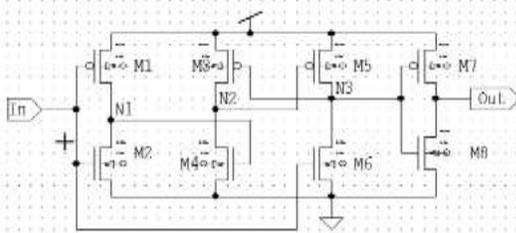


Figure 1: 8-Transistor LS based on Current Mirror

In Figure 2, we can see an LS circuit that uses inverters. The circuit's operation is as follows: At a logic 0 input, M1 is disabled and M2 is enabled. Furthermore, logic 1 will be charged by node N1. Upon reaching logic 0, the output node will release its charge and M4 will activate. Both M1 and M2 will turn on, and node N1 will charge to logic 0 when the input is logic 1. In turn, this activates M3 and raises the logic value at the output node.

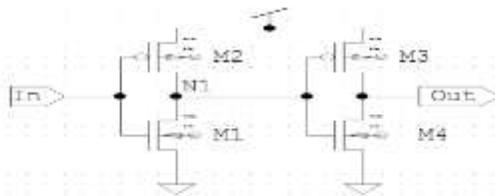


Figure 2: Level Shifter based on inverters

Figure 3 displays the current LS circuit. The circuit works in the following way: At logic 0 input, node N1 charges to logic high and activates M2. My current situation prevents me from taking part in M1. The voltage will increase when M3 is activated and M4 is off. Upon receiving logic 1 input, Node N1 will discharge to logic low and M2 will be deactivated. Just a heads up, M1 is on. The voltage will rise when M3 is disabled and M4 is enabled.

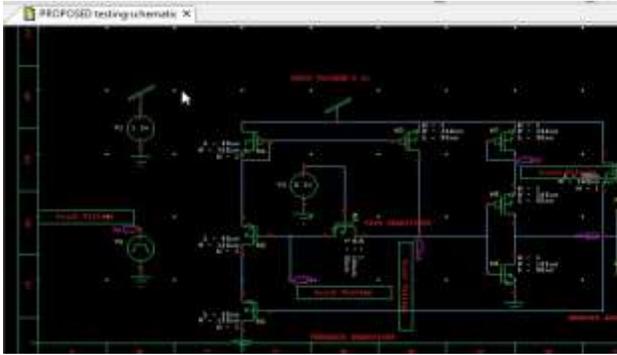
The output voltage may fluctuate between 1.8 and 1.9 volts when the source voltage is 1 volt. Difference in voltage between 1 volt and 1.8 volts. Figure 6 shows information on inverter-based LS. The output waveform, shown in Figure 7, is the result of an LS simulation that makes use of an inverter. Bringing together logic 0 and logic 1 One way to change the voltage is via a level up

shifter. The features of the level shifters are examined in this research using the Cadence virtuoso tool & 180nm technology. The area of 8-transistor LS based on a current mirror is 235.03 pW. With a delay of 60.75 ms, An LS-based inverter has four transistors and an average power of 89.03 pW. A lag of 310.5 ps is seen.

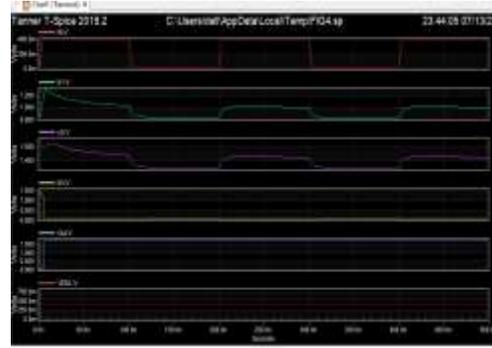
IV. PROPOSED METHOD SIMULATION

The suggested LS for the L→H transition are shown in Figure 5 (a). To create the mirror current via M5, it is possible to activate M2 when IN is high. Once n1 is charged by the mirror current, the discharge of n3 via M6 causes the output to become high. Turning off node M1 and using nodes M2 and M4 to discharge node n3 lowers the static current at node n1. The reduced-swing buffer's diode-connected transistor M7 accomplishes the same thing at node n2 as it does at node n1, according to the suggested LS's simulated behavior. Thus, the suggested LS achieve lowest standby power and remove the excess static current flowing via M8.

The suggested LS for the H→L transition are shown in Figure 5(b). By deactivating M2, the mirror current is stopped, and by activating M3, the pass transistor is activated, resulting in a rapid discharge of n1. When the reduced-swing buffer charges n3 to VDDH using M9, the output drops. The simulation results for the proposed LS and WCMLS are shown in Figure 7. The suggested LS have a much faster fall transition delay when using the pass transistor in conjunction with M9.



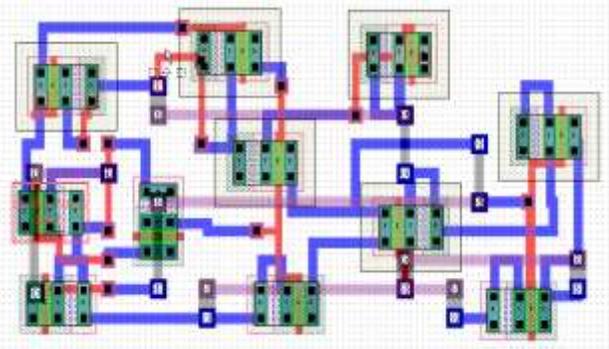
A novel decreased swing buffer (M6-M11) has the potential to stack a diode-connected transistor (M7) at high productivity, hence reducing the enormous static current via M8. The voltage swing correction is finished at node n3, which further accelerates the fall transition, by M9. The proposed LS employ a single pass transistor (M3) and omits an input inverter to further accelerate the fall transition. In order to sidestep the charge sharing issue in WCMLS and the large static current at high output from the current mirror, we place the feedback transistor (M1) between M2 and soil. In the 2000s, pass transistor logic (PTL) emerged as a low-power, high-speed, and small-area substitute for complementary metal-oxide-semiconductor (CMOS) logic. The transfer gate logic (TGL) and dual-value logic (DVL) [2-8] are shown in Fig. 1. It is possible to build pass transistor circuits using specialized NMOS and PMOS transistors. In a transmission gate (TG), two NMOS and one PMOS device are arranged in parallel.



For the sake of comparison, a 65 nm CMOS test chip was programmed with an LS and WCMLS [5]. As predicted, the LS configuration is shown alongside the microphotograph of the test chip. The experimental results show that the proposed LS can raise the voltage from below the threshold—1.2 V—down to 100 mV. After converting 200 mV to 1.2 V, Figure 9 shows the waveform that the suggested LS detected.

In contrast to the anticipated LS delays of 1.2 V ($V_{DDH} = 1.2$ V), with V_{DDL} being swept, the measured WCMLS delays range from 0.3 V to 1.0 V, as seen in the figure. Because of the pass transistor and M9, the provided LS can function from 0.3 V to 1.2 V with a latency that is 2.3 times faster than WCMLS. For V_{DDL} values between 0.6 V and 1.0 V, the proposed LS outperform WCMLS in terms of latency by a factor of up to 2.7 \times .

V. PROPOSED METHOD LAYOUT



At $V_{DDH} = 1.2$ V, the figure displays the leakage power of the two LSs as a function

of VDDL. The results of the leakage power test at VDDL = 0.6 V demonstrate that the suggested LS achieves a maximum leaking decrease of 16.3× when compared to WCMLS. Leakage has been successfully improved thanks to the suggested reduced-swing buffer design.

COMPARISON TABLE

VI. CONCLUSION AND FUTURE SCOPE

Utilizing 180nm technology and the Mentor Tanner tool, this research delves into the investigation of the level shifters' operations. With 11 transistors, the LS have an area of 235.03 pW and an average power derived from the current mirror. An LS-based inverter has four transistors and an average power of 89.03 mW. There is a 310.5 ms lag. Eleven transistors, 2.0730e-09 area, and 2.055e-07 average power make up the proposed LS. At 1.417e-05, its static power is high. The proposed LS have further advantages when considering overall performance. A level shifter is often located on a SIM, audio, SD, UART, or CF card. With only one supply level shifter, we were able to cut power usage by 45% and delay by 50%. This improves the system's overall performance by making it simpler and cheaper.

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S	Me	A	M	Mi	No
1	Exi	1.	2.	1.6	4
2	Pas	2.	1.	2.0	11

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