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A study of Power Consumption Using High-Speed and Low-Power Comparator advanced ADC

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ABSTRACT

Today, the high performance of electronic equipment is dependent on the development ofhigh-speed analog to digital converter (ADC). And, the most common structure of high-speedADCisFlashADC.ThedesignofcomparatoristhemostcriticalpartintheFlashADC, since the speed and the resolution of Flash ADC is determined by the comparator. Inthis paper, a high-speed low-power comparator, which is used in a 2 Gsps, 8 bit Flash ADC,is designed and simulated. Based on 0.18 um TSMC CMOS process model, the comparatorcircuitissimulatedwitha1.8VpowersupplyinCadenceenvironment.Theresultshowsth atit can work at a 2GHZ clock frequency, and the dynamic power consumption is only 1.2mW,with123.5pstransmissiondelay.Inaddition,theaverageoffset voltageofthiscomparatorisonly 676.3uV, which can meet the requirements of an 8-bit Flash ADC.There have threetypes of comparator can provide the high speed, such as multistage open loop comparator,the dynamic latch comparator, and the preamplifier-latch comparator. The multistageopenloop comparator can meet high-speed and high-precision, but it is hardly can provide thespeed more than 1Gsps.The dynamic latch comparator is widely utilized to satisfy the needfor high-speed. However, this kind of comparator has large offset voltage which affects theresolution of Flash ADC. The preamplifier-latch comparator can obtain high-speed and high-resolution because of its circuit structure. In this paper, by considering factors of speed andresolution,preamplifier-latchcomparatoristhechoiceforFlashADC.

1. Introduction

Lower power consumption and higher bandwidth are wthe two dominant requirements in designing next-generationhigh-end applications. The global trend across multiple marketsis for higher bandwidth in the same footprint at the same orlowerpowerandcost. The Internetisgoing mobileand video is driving bandwidth requirements at a growth rate of 50% yearon year. The march to 40G and 100G systems (with 400G onthehorizon)isunderwaytosupportthisever-growingbandwidth demand. Fierce competition is driving down prices.Spaceconstraintsabound,andcoolingsolutionsoftendomina te the power budget, sometimes up to twice the powerconsumption of the electronics. The next generation of 28-nmhighendAlteraFPGAsaddressesthesechallengesthroughleadin g-edge technological innovation, integration, and reducedpowerconsumption.Designingnext-generationFPGAstoaddressthecurrenttrendofhigherbandwidthan dlowerpoweris becoming much more challenging. Many factors must becarefullyconsideredwhenplanninganewFPGAfamilytoensureth enewdevicescanaddressthepowerandperformancerequirements ofthetargetedapplicationsinvarious market segments. These factors include selecting therightprocesstechnology,designingtherightarchitecture,applyi ng the right software power optimization, and enablingeasier and power-efficient system-level design. Altera took aholistic approach in designing Stratix V FPGAs to deliver thelowestpowerand highest bandwidthFPGAs in the industry.Key innovations were introduced at various levels to optimizetheStratix VFPGAs'powerand performance for designerslookingtobuildahigher bandwidthdesignwhilereducingthermalpowerconsumption(Figure1).

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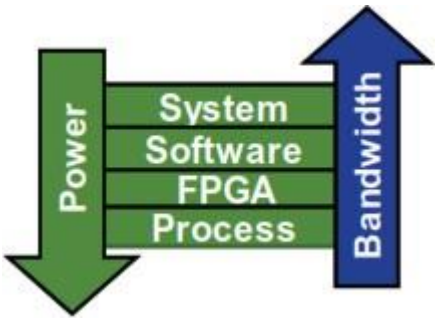


Figure1.Altera'sHolisticApproachtoReducePowerandIncreaseBandwidth

2. Power Consumption In High-End FPGA Designs

There are three components to power consumption: static,dynamic,andI/Opower.

StaticPower

Staticpoweristhepowerconsumedbythe FPGAwhenno signals are toggling. Both digital and analog logic consumestatic power. The sources of static leakage current in 28-nmtransistorsareshowninFigure2andTable1.

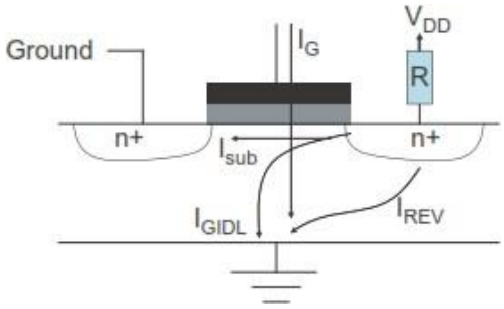


Figure2.SourcesofTransistorLeakage

Table1.MainSourcesofTransistorLeakage

Main Sources of Leakage	Impact	Mitigation Techniques
Subthreshold leakage (I_{sub})	Dominant	■ Lower voltage ■ Higher voltage threshold ■ Longer gate length ■ Dopant profile optimization
Gate direct-tunneling leakage (I_G)	Dominant	High-k metal gate (HKMG)
Gate-induced gate leakage (I_{GIDL})	Small	Dopant profile optimization
Reverse-biased junction leakage current (I_{REV})	Negligible	Dopant profile optimization

Dynamic Power

Dynamic power is the additional power consumed throughthe operation of the device caused by signals toggling andcapacitive loads charging and discharging. As shown in Figure3, the main variables affecting dynamic power are capacitancecharging, the supply voltage, and the clock frequency. DynamicpowerdecreaseswithMoore'slaw bytakingadvantageofprocessshrinkstoreducecapacitanceandvolt age.Thechallengeisthatasgeometriesshrinkwitheachprocessshrin k,themaximumclockfrequencyincreases.Whilethepower reduction declines for an equivalent circuit from processnode to process node, the FPGA capacity doubles and themaximumclockfrequencyincreases.

$$P_{dynamic} = \left[\frac{1}{2}CV^2 + Q_{ShortCircuit}V\right]f \cdot activity$$

Capacitance charging — Short circuit charge during switching — Percent of circuit that switches each cycle

Figure3.VariablesAffectingDynamicPower

I/OPower

I/O power includes the power consumption consumed byI/Oblocks,includinggeneral-purposeI/Osandhigh-speedserialtransceivers.Themainfactorsimpactinggeneral-purpose I/O power consumption are shown in Figure 4 andsummarizedinTable2.

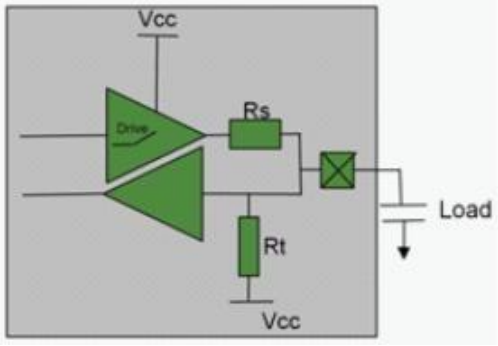


Figure4.FactorsImpactingGeneral-PurposeI/O Power

Table2.MainFactorsImpactingGeneral-PurposeI/O Power

Main Factors Impacting I/O Power	Mitigation Techniques
Termination resistors (on-chip series termination (R_S OCT) and on-chip parallel termination (R_T OCT))	Dynamic on-chip termination (DOCT)
Output buffer drive strength	Programmable drive strength
Output buffer slew rate	Programmable slew rate
I/O standard (single ended, voltage referenced, or differential)	Support for multiple I/O standards
Voltage supply	Support for various voltage rails
Capacitive load (charging/discharging)	Interface dependent

Themainfactorsimpactingthepowerconsumptionofhigh-speedserialtransceiversinclude:

- Datarates(Gbps)
- Pre-emphasisandequalizationsettings
- Interfaceload(chip-to-chiporchip-to-backplane)
- Transceivercircuitdesign

Figure5showsthebreakdownoftotalpoweracrossvarious high-end FPGA customer designs. Dynamic and I/OpowerdominatetheFPGA'stotalpowerconsumption.Because high-end FPGA designs tend to push the envelope in terms ofbandwidth and performance, they use more logic running at ahigher clock fMAX. With I/Os toggling at higher data rates andlogictogglingatfasterfrequencies,thecharginganddischarging ofloadsonandoffchipbecomesthemainconsumer of FPGA power. To effectively reduce total FPGApower,both staticand dynamicpowermust be addressedwhileensuringtheFPGA'sperformancestillmeetsdesignr equirements.

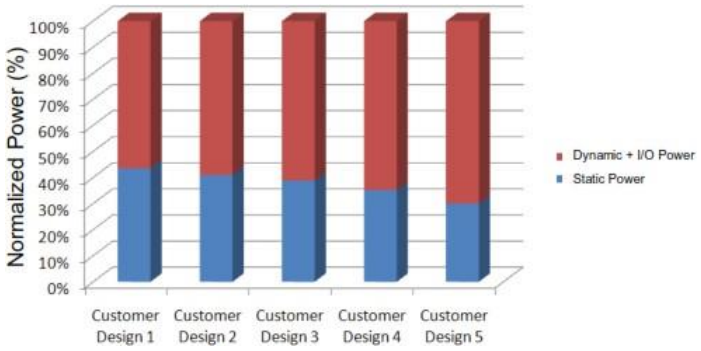


Figure5.TotalPowerBreakdownacrossVariousHigh-EndFPGACustomerDesigns

3. Structure of Pre amplifier-Latch Comparator

A comparator, by definition is 'a circuit that compares thetwo analog input signals and decodes the difference into asingledigitaloutputsignal'[4].Thepreamplifier-latchcomparatorisconsistingofpreamplifier,regenerativelatchcomparator and an output latch. The preamplifier's role is toamplifyinputanalogsignals.Then,theregenerativelatchcomparatorcomparestheenlargedsignalsfromthepreamplifier. As the last stage, output latch deals with theresults from the regenerative latch comparator, and generatesthedigitallevel(1or0)asthefinaloutputofcomparator.Inthepreamplifier-latch comparator, the main roles of preamplifier:firstly,itcanamplifytheinputsignalstoreducethecomparisontime of regenerative latch comparator so as to improve thespeedofcomparator;inaddition,italsocanamplifythedifferential inputsignalstoreducetheinfluenceoftheoffset voltage. Therefore, the preamplifier should have a high gainand a wide bandwidth. In general, in order to improve thespeed of comparator, the first choice for latch comparator isregenerativeloopstructure[5].Theregenerativelatchcompared input signals by a positive feedback. It can quicklyamplified input signals to improve the speed [6]. In order tohave a stable digital level, it is better to add an output latchafter the regenerative latch comparator. So output latch is thelast stage of comparator, and the final output will be generatedbyit[7].Whentheregenerativelatchcomparatorisinthereset mode, output latch will keep the level of the last clock period.Outputlatchwillgeneratethefinaloutputwhentheregenerativelatchcomparatorisinthecomparemode.

Theoverallschematicofthehigh-speedandlow-power comparatorisshowninFig6.

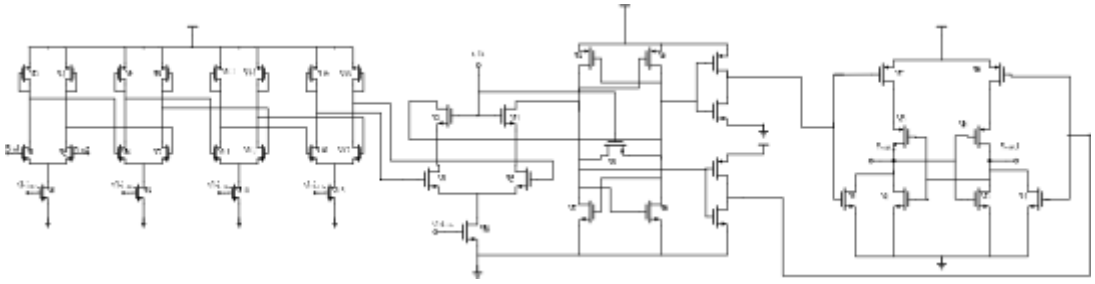


Fig.6TheOverall Comparatorcircuit

4. Optimization of Comparator

1.Optimization of Pre amplifier

To get high bandwidth and high gain, the preamplifierneedsmultistageamplifiers.Butwiththeincreaseofstages,the transmission delay will increase, and the offset voltage alsoincreases. Meanwhile,the layout area and power consumptionincrease.Therefore,itisveryimportanttoselectthenumberofstagestoreducethedelayofpreamplifier.Thedelayofpreamplifiercanbeexpressedbyequation(1):

$$t = n\tau = \frac{n \cdot A^{\frac{1}{n}}}{G \cdot BW} = \frac{1}{G \cdot BW} \cdot n \cdot A^{\frac{1}{n}} \quad (1)$$

Where, t is the delay of preamplifier, n is the number ofamplifiers, r is the delay of each amplifier, A is the gain ofpreamplifier,Gisthegainofeachamplifier;BWisthebandwidth of each amplifier. Fig 7 shows the simulation resultsof equation (1) with Matlab software tools. In Fig 8, X axisdescribesthenumberofamplifiersn,Yaxisexpressestotal gain A, Z axis shows the transmission delay of preamplifier t.Fortheminimumoftransmissiondelay,nisbesttobe2,3or

4. What's more, the preamplifier must have enough gain toamplify the input signals and to reduce the offset voltage ofcomparator.Consideringfactorsofgainandtransmissiondelay, the preamplifier should be consisting of 4 stages ofamplifierwhosegainisaboutconstante.

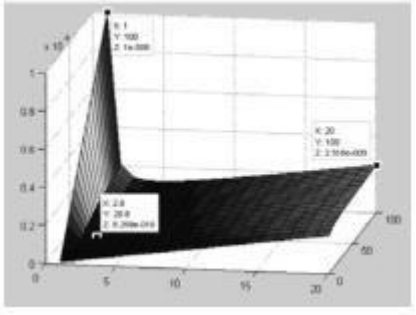


Fig.7SimulationResultsofEquation(1);

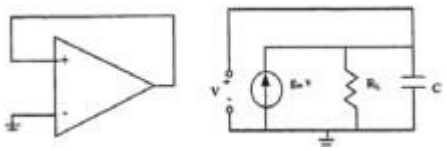


Fig.8The smallsignalmodel

2.Reduce the delay of Regenerative Latch Comparator

Theregenerativelatchcomparatorusesthepositivefeedback and amplifier to realize the comparison of two inputsignals.AsshowninFig8,thesmallsignalmodelofregenerative latch comparator is from an amplifier with positivefeedback[8].Accordingtothesmallsignalmodel,thetransmissiondelaycanbeanalyzedasfollows:

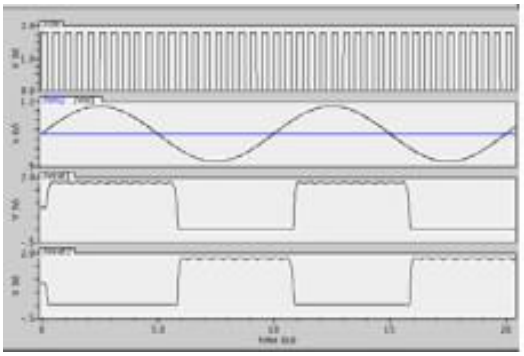
$$g_m V = \frac{V}{R_L} + C\frac{dV}{dt} \quad (2)$$

Where,Cisthetotalcapacitance,includinginputcapacitance and output capacitance. From the integration ofequation(2),thetransmissiondelaytimeisasfollows:

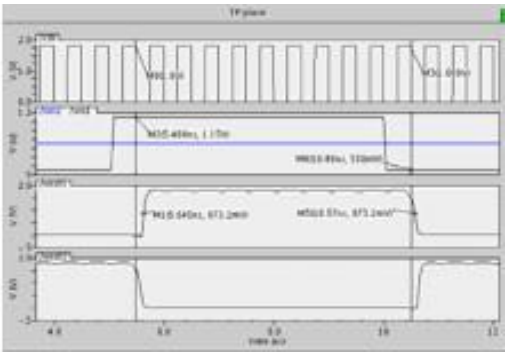
$$\Delta t = t_2 - t_1 = \ln\left(\frac{V_2}{V_1}\right)\cdot\frac{C}{g_m}\left(1+\frac{1}{g_m R_L - 1}\right) \quad (3)$$

5. Simulation Results

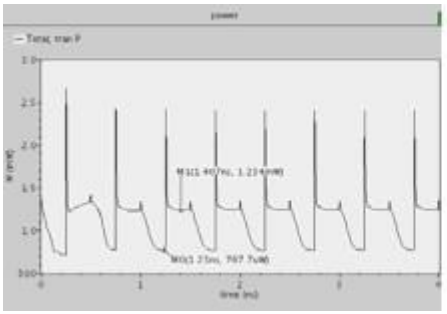
Based on TSMC 0.18um CMOS process model, the high-speed and low-power comparator is simulated with Spectre ofCadence. The comparator's clock frequency is 2GHZ, and thevoltage of powersupply is 1.8V.Firstly,thereisthe logicsimulationresultofthepreamplifier-latchcomparatorinFig9 (a) .When vin1 is bigger than vin2, the output terminal vout1 isathighlevel,andvout2isatlowlevel.Secondly,thetransmission delay of comparator is shown in Fig 9 (b). It isseen that the transmission delay between input and outputsignalsisabout123.5ps.Thesmalldelaycanmakethecompar atorworknormallyunderthehigh-frequencyclock.Thirdly, the power consumption of comparator is simulated, asshown in Fig 9 (c). When the regenerative latch is in the resetmode,thestaticpowerconsumptionofthewholecomparatoris only767.7uW.Butwhentheregenerativelatchisinthecompare mode, the dynamic power consumption of the wholecomparator is about 1.234mW. Therefore, the average powerconsumptionisabout1mW.Andthen,thecomparatorissimula ted for 200 times Monte Carlo, and the offset voltagesimulation result is shown in Fig9 (d). The offset voltagedistributes between -1.5 mV and + 2 mV, and the averageoffsetvoltageisonly676.3uV.

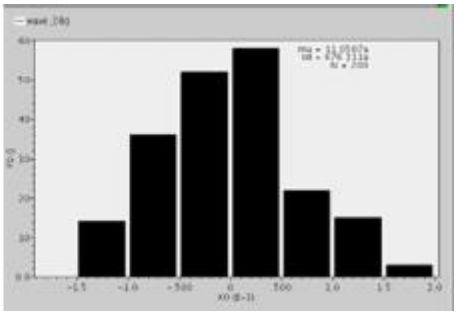


(a) logicsimulationofcomparator;



(b)transmissiondelayofcomparator





(c)powerconsumptionofcomparator;(d)offsetvoltageofcomparatorFig.9Sim ulationResults

6. Conclusion

Thispaperproposedahigh-speedandlow-powercomparator in Flash ADC. Due to increase the speed of thecomparator,thispaperoptimizesthepreamplifierandtheregene rative latch comparator. The results show that it canworkata2GHZclockrate,andthetransmissiondelaytimeis only 123.5ps. What's more, the average power consumption ofthis comparator is about 1mW.The comparator can be used inFlashADCbecausethattheaverageoffsetvoltageof thecomparatorisonly676.3uV.

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