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RECONFIGURABLE VLSI DIGITAL FILTERS FOR TOLERATING MULTIPLE TIMING ERRORS

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ABSTRACT

One of the major problems with advanced semiconductor technology is timing errors caused by process variation and device aging. With such problems, conventional worst-case designs suffer poor system performance. This paper proposes an aggressive design technique for VLSI digital filters for tolerating timing errors. When a timing error occurs, the system reconfigures the buffer cell of the problematic stage with little performance degradation. We have applied the technique to several digital filters. The design of an IIR filter with tolerance of timing errors is described and demonstrated. The results show that our proposed design achieves tolerance of multiple timing errors with small cost of chip area and power consumption.

KEYWORDS—timing errors; digital filters; reconfigurable architectures; VLSI design; error-resilient circuit design

I. INTRODUCTION

Integrated circuits are more and more susceptible to process variation and device aging with advanced semiconductor technology. It is more difficult to predict the timing behavior of the system due to delay variation of circuits [1,2]. Most current designs of integrated circuits are based on the worst-case scenario. Such conservative designs consider all possible delay variation in order to guarantee safe system operations. However, this conventional approach results in poor system performance. Hence, aggressive methodologies have been proposed for robust system design which can tolerate timing errors [3,4,5,6,7].

In the Razer project, better-than-worst-case design was proposed for processor pipelines

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with double sampling of data signals [5]. When a timing error occurs, the whole pipeline is halted for a clock cycle. However, halting the whole pipeline for a clock cycle hurts the pipeline performance. T-error is another research work that deals with error-resilient link design in network-on-chip architectures [6,7]. With similar double sampling technique, the design in T-error can tolerate timing errors for network links. However, their approach is only for tolerance of transmission link errors.

In this paper, we propose the robust design of reconfigurable VLSI digital filters with tolerance of multiple timing errors due to process variation and device aging. In the next section, the design technique of error-resilient VLSI digital filters for tolerating timing errors is presented. With such design, timing errors occurring to digital filters can be tolerated efficiently. The design and implementation of a timing-error-resilient IIR digital filter are described in Section III. The summary and conclusions are given in the final section.

II. Reconfigurable Design for Tolerating Timing Errors

Process variation and device aging problems may cause timing errors for advanced VLSI circuits. When timing errors occur, the latches or registers in the circuits may get the instable or wrong data signals due to not sufficient delay of the clock cycle. One of the design techniques for tolerating timing errors is to use double sampling of input data [6,7]. Besides the main clock, there is a delayed clock to sample the input data, which has sufficient time to catch the correct data when there is a timing error for the main clock. Fig. 1 shows the buffer cell for tolerating the timing error.

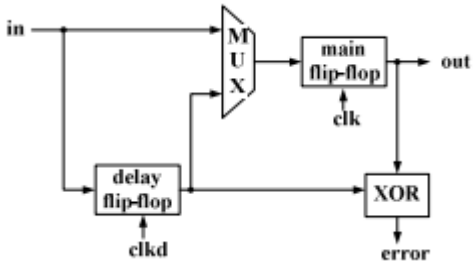

Fig. 1 Buffer cell for tolerating the timing error.

There are two flip-flops in the buffer cell in Fig. 1: main flip-flop and delay flip-flop. The main flip-flop samples the input data at the edge of the system clock clk, while the

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delay flip-flop does that at the edge of the delay clock clkd.

The clock edge of clkd arrives later than clk by a portion of one clock cycle, e.g. two thirds or three fourths of a cycle. When a timing error occurs, the data written into the main flip-flop is incorrect due to not sufficient cycle time. However, the delay flip-flop is able to catch the correct data. With the XOR gate to indicate the occurrence of the timing error, the cell enters the delay mode from regular mode in our design. When in the delay mode, the cell uses the output of the delay flip-flop instead of the in through the multiplexer as the input data for the main flip-flop. Note that there is an invalid data sent out to the output before the correct one.

We can aggregate a group of the above buffer cells to compose a buffer stage for the digital filter [6,7]. For example, if the datapath is 16 bits wide, then a buffer stage of the datapath consists of 16 buffer cells. The error signals from the cells in the same stage are OR'ed together and the output signal is sent to the corresponding control circuit to indicate there is a timing error in this stage. The control circuit directs the multiplexers in the corresponding stage. The control circuit also informs the downstream stage whether the data sent is valid or not for the timing error. In our reconfigurable digital filter design, there are two operating modes, regular mode and delay mode, in each stage of the digital filter.

The system starts out with each stage buffer with regular mode. When a timing error occurs in any stage, the stage buffer is reconfigured and changes from regular mode to delay mode. In the delay mode, each incoming data spend two clock cycles to go through this stage. Furthermore, the control circuit will inform the downstream stage that a timing error occurs and the data transmitted is invalid.

III. Design and Implementation of Error-Resilient Reconfigurable Digital Filters

One of the challenging issues of designing error-resilient digital filters is how to ensure each data meets the other associated data at the correct stage. Otherwise, the output data would be incorrect. We have developed a design methodology of designing reconfigurable digital filter for tolerating timing errors. Our proposed design

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technique can tolerate any number of timing errors occurring at any stage anytime.

We have applied our design technique in the above to several digital filters for tolerating timing errors.

In the following, we demonstrate the design of a 3-parallel 2nd-order IIR filter among them. The implementation results are also shown for both the original IIR filter and the error-resilient filter to evaluate the performance and cost. Fig. 2 shows the logic design of this 3-parallel 2nd-order IIR filter. For the error-resilient design of this digital filter, the pipeline buffer (PB) is redesigned with 2 flip-flops in each buffer, and the corresponding control circuit for each buffer in different stages is included in the PB. The main purpose of the revised control circuit is to reconfigure the stage when the timing error occurs, and to coordinate with related stages.

We have implemented this example digital filter for both original design and error-resilient design with 8-bit and 16-bit data width using cell-based design flow. TSMC 90nm technology is used in our design. In order to make the design work, some padding circuits are added in the datapath, such that the filter can operate correctly when some of the filter stages encounter timing errors and enter the delay mode. Table I and Table II show the implementation results for the IIR filter. Our results demonstrate that our error-resilient designs achieve tolerance of timing errors with reasonable area cost. Note that the circuit speed of the error-resilient designs is the same as the original designs. The reason for this is that the multiply and add operation in the combinational circuit dominate the clock cycle, and the delay of the extra circuit in the error-resilient design is so small and negligible.

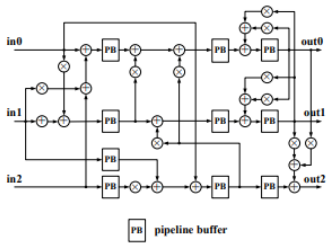

Fig. 2 Design of the 3-parallel 2nd-order IIR filter.

TABLE I Implementation results for the IIR with 8-bit data width

	Original IIR	Error- resilient IIR
Clock rate	89.3 MHz	89.3 MHz
Area of core	21,572 μm^2	26,950 μm^2
Power consumption	0.90 mW	1.10 mW

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TABLE II Implementation results for the IIR with 16-bit data width

	Original IIR	Error- resilient IIR
Clock rate	64.9 MHz	64.9 MHz
Area of core	39,153 μm^2	47,073 μm^2
Power consumption	1.98 mW	2.31 mW

IV. SUMMARY AND CONCLUSIONS

This paper presents an aggressive design technique for Reconfigurable VLSI digital filters for tolerating multiple timing errors. When the timing error occurs, the system reconfigures the buffer cells of digital filters with little performance degradation. The implementation results show that our proposed designs achieve tolerance of multiple timing errors with reasonable cost.

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