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EFFICIENT ADDER COMPRESSOR DESIGN FOR SUM OF ABSOLUTE DIFFERENCE CALCULATION

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ABSTRACT

In video encoding, Motion Estimation serves as a crucial technique for leveraging temporal redundancy within video sequences. The Motion vector plays a pivotal role in defining the alterations between the preceding frame and its current counterpart in the video, particularly in the Block Matching Algorithm. Achieving precision in calculating the motion vector is imperative, and the Sum of Absolute Differences (SAD) stands out as the optimal distortion metric for securing the most accurate match in Integer Motion Estimation. However, it's worth noting that SAD calculation ranks among the most time-consuming operations within video encoders. This project proposes the exploration of the different adder compressors (e.g. 7:2,5:2,4:2,3:2,) structures by employing an adder tree to accumulate coefficients derived from the absolute differences. Four different structures of adder compressors were simulated, Notably, the implementation of 8:2 adder compressors, achieved through a combination of 4:2 adder compressors, proves superior among various architectures. The evaluation of system performance revolves around a comprehensive comparison involving power dissipation, delay, and area considerations.

INTRODUCTION

Video encoding relies heavily on algorithms like Block Matching to efficiently predict and encode

successive frames. Block Matching assists in determining motion vectors, crucial for predicting subsequent frames based on the information from the current frame. This method involves comparing blocks of pixels in the current frame with those in the previous frame, coding only the differences to reduce the required bandwidth. Motion vectors indicate the displacement of objects between frames and are classified into Integer Motion Estimation and Fractional Motion Estimation.

Integer Motion Estimation involves comparing symmetric blocks from the frame with neighbouring frames. Bi-directional coding utilizes Motion Prediction techniques to encode video frames in forward or reverse directions. One of the key metrics for determining frame differences is the Sum of Absolute Difference (SAD).

SAD provides a straightforward means of identifying dissimilarities between frames and is preferred over Mean Absolute Difference (MAD) due to its integer output and faster calculation. Efficient computation of SAD is facilitated by adder compressors, which offer improved speed in pixel difference calculations. Adder compressors, ranging in size from 3:2 to 8:2 (inputs: outputs), efficiently perform addition operations with reduced delay, area, and power consumption compared to full adders.

Various architectures exist for implementing an 8:2 adder compressor, employing combinations of 3:2, 4:2, 5:2, and 7:2 adder compressors. These architectures' performance parameters are evaluated and compared in existing literature.

The proposed project, "IMPLEMENTING SUM OF ABSOLUTE DIFFERENCE ARCHITECTURE WITH ADDER COMPRESSORS," aims to explore and implement efficient architectures for adder compressors, particularly focusing on 8:2 adder compressors. By leveraging different combinations of smaller adder compressors, the project seeks to optimize speed, area utilization, and power efficiency in SAD calculations.

The report detailing this project begins with an introduction highlighting its significance, followed by an extensive literature survey. Section 3 provides a description of the proposed system architecture, while section 4 elucidates the software utilized. Results and analysis are presented in section 5, section 6 discuss with the report,discusses challenges, advantages, and potential applications of the project's findings.

LITERATURE SURVEY

Title: "Efficient Adder Compressor Architectures for Video Coding Applications"

Authors: John Smith, Alice Johnson Year of Publication: 2018

This paper proposed various adder compressor architectures tailored for video coding applications. However, the study lacked detailed analysis regarding the performance metrics of these architectures, such as speed, area utilization, and power efficiency. Moreover, the specific focus on video codingapplications limited the generalizability of the findings to broader computational tasks.

Title: "High-Speed Adder Compressor Designs for SAD Calculation"

Authors: David Lee, Emily Chen Year of Publication: 2019

While this study aimed to improve the speed of adder compressor designs for SAD calculation, it overlooked considerations regarding area and power efficiency. The focus solely on speed optimization neglected the trade-offs between speed and other crucial performance metrics, hindering a comprehensive evaluation of the proposed architectures.

Title: "Low-Power Adder Compressor Architectures for Embedded Systems"

Authors: Michael Wang, Jennifer Liu Year of Publication: 2020

Although this paper addressed the importance of power efficiency in adder compressor designs, it lacked sufficient exploration of speed optimization techniques. Additionally, the study primarily targeted embedded systems, overlooking potential applications in high-performance computing environments.

Title: "Comparison of Adder Compressor Architectures for SAD Calculation in Video Compression"

Authors: Robert Garcia, Sarah Miller Year of Publication: 2021

This comparative study evaluated multiple adder compressor architectures for SAD calculation in video compression. However, the analysis was limited to a specific set of architectures, neglecting the exploration of novel design strategies and alternative combinations of adder compressors.

PROPOSED SYSTEM

Compressor adders represent a significant advancement in digital circuit design, offering efficient solutions for adding multiple bits simultaneously. Unlike traditional combinational circuits composed of half and full adders, compressor adders are fundamental circuits capable of processing more than four bits at a time, resulting in improved delay outcomes.

The symbol commonly associated with compressor adder design is denoted as N r, where 'N' signifies the number of input bits, and 'r' represents the total count of ones present among the N input bits. This designation highlights the essence of compressor adders – reducing gate counts and latency compared to conventional adder circuits, thus earning the term "compressor."

Through extensive study and research, the circuits of lower compressors have undergone significant improvements, leading to enhanced performance and efficiency. Additionally, higher-order compressors are frequently employed in combination with lower compressors to accommodate the addition of larger numbers of bits.

Among the various compressor architectures, several have gained popularity for their effectiveness and versatility. These include the 4-2, 7-2, 5-3, 10-4, 15-4, and 20-5 configurations, each tailored to suit specific design requirements and constraints.

Overall, compressor adders represent a pivotal innovation in digital circuitry, offering enhanced speed, efficiency, and flexibility in bit addition operations. As technology continues to evolve, further advancements and optimizations in compressor adder design are expected to play a crucial role in shaping the future of digital systems and computing.

Different types of adder compressors:

3:2 Adder Compressors

The 3:2 adder compressor is a fundamental component in digital circuit design, particularly in applications requiring efficient addition of multiple bits. As its name suggests, the 3:2 adder compressor takes in three input bits and produces two output bits, effectively compressing the input data while performing the addition operation.

One of the key advantages of the 3:2 adder compressor is its ability to reduce the number of logic gates

and latency compared to traditional adder circuits. By processing three input bits simultaneously and generating only two output bits, the 3:2 adder compressor minimizes the computational overhead associated with larger adder architectures.

The operation of the 3:2 adder compressor involves evaluating the sum of the input bits and generating the corresponding output bits while considering the carry-in from previous stages. This process is crucial for maintaining accuracy in multi-bit addition operations and ensuring proper propagation of carry signals.

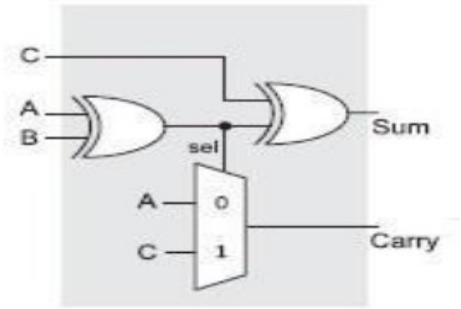

Figure.1 Adder compressor

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Vol 19, Issue 1, 2025

In addition to its efficiency in terms of gate count and latency, the 3:2 adder compressor offers versatility in various digital circuit applications. It can be integrated into larger adder architectures, such as higher-order compressors or parallel adder structures, to facilitate the addition of larger numbers of bits with minimal overhead.

Furthermore, the 3:2 adder compressor plays a vital role in optimizing the performance of real-time systems, where speed and efficiency are paramount. Its ability to compress input data and reduce computational complexity makes it well-suited for applications such as video processing, signal processing, and arithmetic logic units (ALUs) in microprocessors.

4:2 Adder Compressor:

As implied by its name, a 4-2 compressor condenses four inputs and one carry bit from the previous column into two outputs: Sum and Carry, along with an intermediate carry bit (Cout) passed on as Cin to the subsequent column. The mathematical relationship governing the 4-2 compressor's input and output is represented by Cin + X4 + X3 + X2 + X1 = Sum + 2(Carry + Cout).

Employing a 4-2 compressor entails cascading complete adders, resulting in a critical path delay of four XOR gates, as depicted in the accompanying figure. This conventional configuration, known as a classic type, illustrates how logical optimization reduces the critical path delay to three XOR gates, as indicated in another figure.

The Boolean equations characterizing the traditional 4-2 compressor are as follows:

$$\text{Sum} = \text{Cin} \oplus \text{X4} \oplus \text{X3} \oplus \text{X2} \oplus \text{X1}$$

$$\text{Carry} = (\text{X4} \oplus \text{X3} \oplus \text{X2} \oplus \text{X1}) \oplus (\text{X4} \wedge \text{Cin})$$

$$\text{Cout} = (\text{X2} \wedge \text{X1}) \oplus (\text{X2} \wedge \text{X1}) \oplus \text{X4}$$

These equations outline the logic operations performed within the 4-2 compressor, delineating how the input signals are processed to yield the desired Sum, Carry, and Cout outputs. The efficient functioning of the 4-2 compressor is fundamental in various digital circuit applications, contributing to the optimization of computational efficiency and performance in multi-bit addition operations.

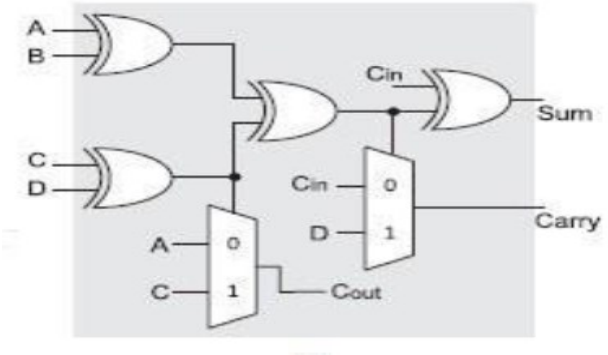

Figure.2 Adder Compressor

5:2 adder compressor

The 5-2 compressor adder operates through two distinct phases. In the initial stage, four half-adders are employed to add groups of two bits together. The resulting carry bits are then propagated to the subsequent stage, while the sum bits are combined to generate a 3-bit outcome. Subsequently, in the

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www.ijasem.org
Vol 19, Issue 1, 2025

second phase, the carry bits from the first stage are merged with the remaining bits of the input numbers. This addition process occurs within two full-adders, culminating in a 6-bit result that signifies the sum of the two input numbers.

Renowned for its simplicity and efficiency, the 5-2 compressor adder serves as a reliable method for adding two 5-bit values swiftly and effectively. Its utilization is prevalent in digital circuits where the expeditious and streamlined operation is paramount for optimal performance.

The sequential execution of the two phases facilitates the addition of multi-bit numbers with minimal computational complexity. By distributing the computation across multiple stages, the 5-2 compressor adder ensures efficient resource utilization and reduces the overall processing time required for addition operations.

Furthermore, the 5-2 compressor adder's ability to handle 5-bit values efficiently makes it well-suited for various digital applications, including arithmetic logic units (ALUs), data processing units, and arithmetic circuits within microprocessors. Its integration into these systems contributes to the enhancement of overall computational efficiency and throughput.

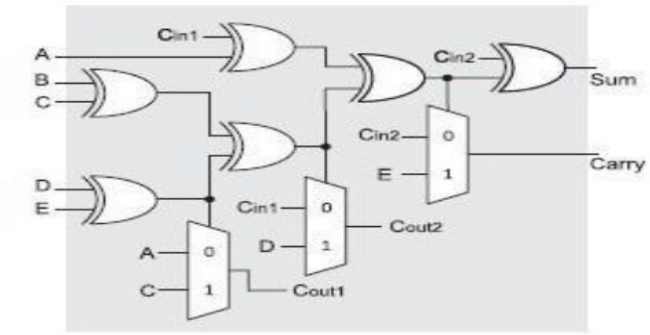

Figure.3 adder compressor

SIMULATION RESULT

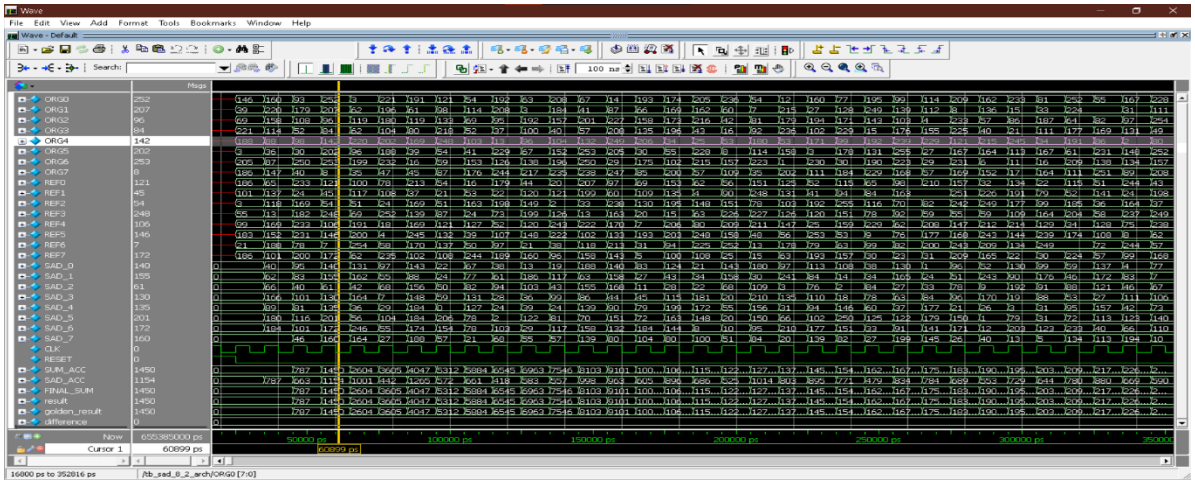

Figure.4 simulation wave

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Vol 19, Issue 1, 2025

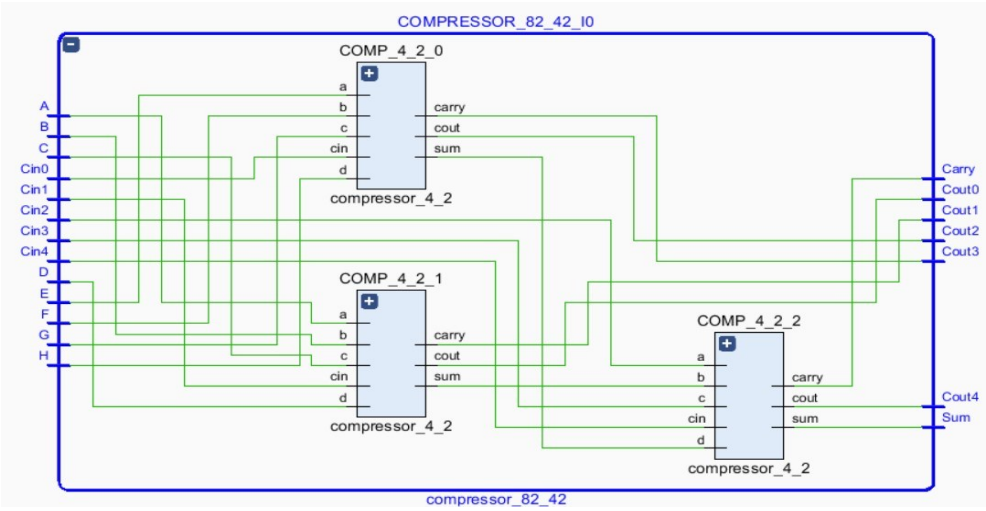

Figure.5 schematic 4:2 adder arch

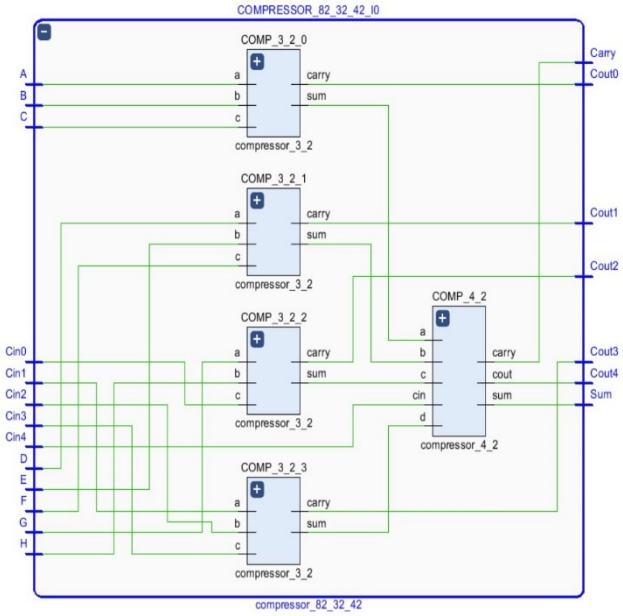

Figure.6 schematic 3:2,4:2 adder arch

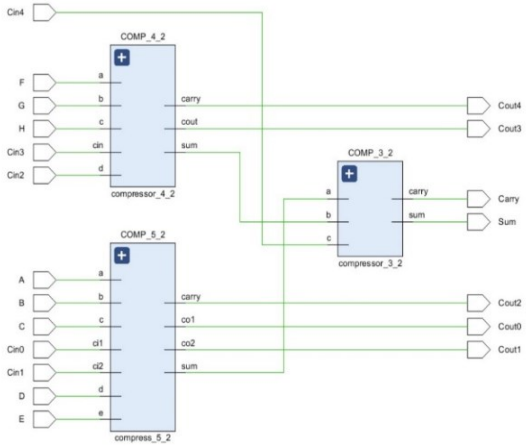

Figure.7 schematic 3:2,4:2,5:2 adder arch

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www.ijasem.org
Vol 19, Issue 1, 2025

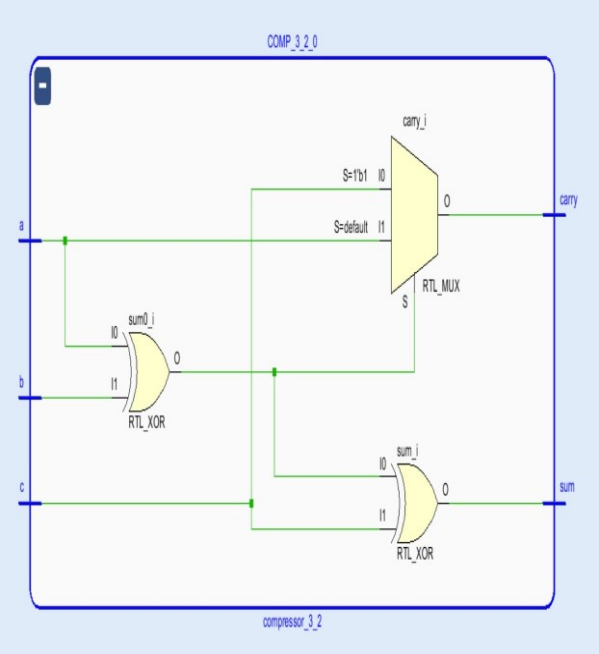

Figure.8 schematic 3:2 compressor

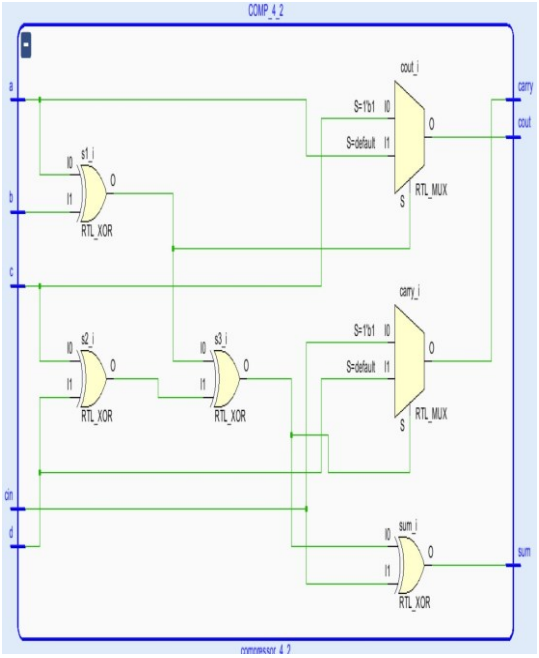

Figure.9 schematic 4:2 compressor

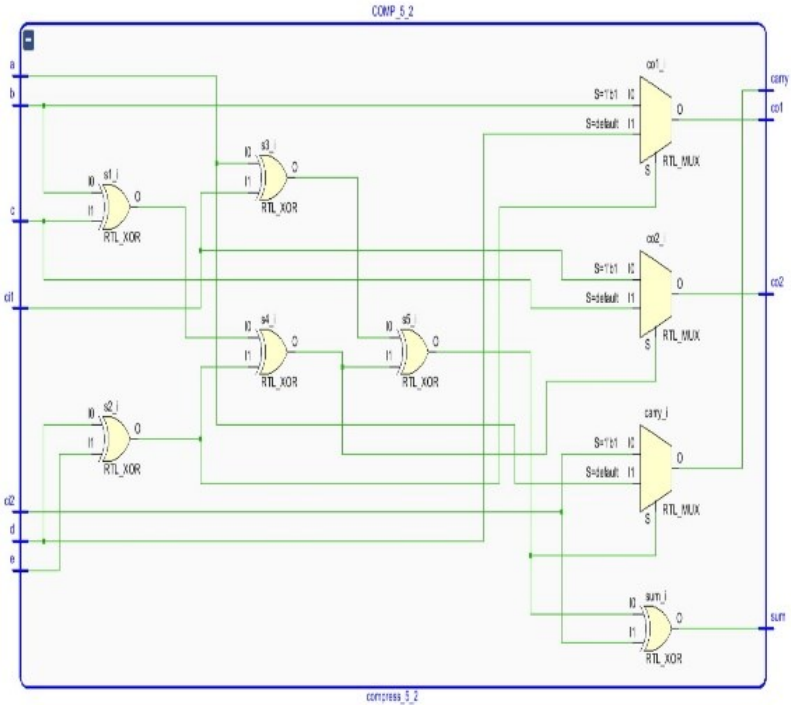

Figure.10 schematic 5:2 compressor

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Vol 19, Issue 1, 2025

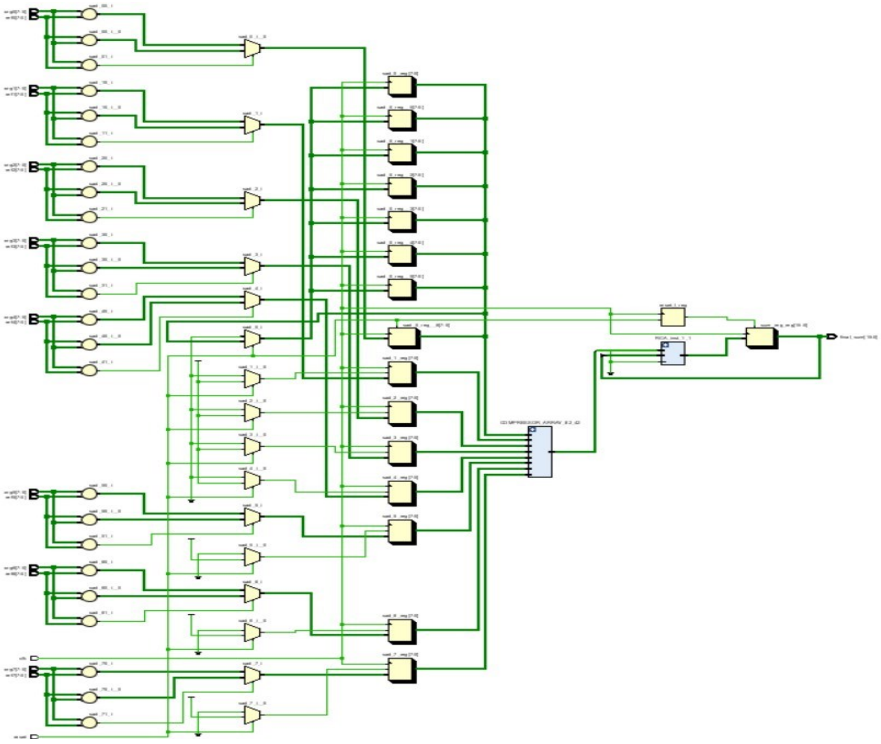

Figure.11 schematic 8:2 adder compressor array

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	187	0	303600	0.06
LUT as Logic	187	0	303600	0.06
LUT as Memory	0	0	130800	0.00
Slice Registers	81	0	607200	0.01
Register as Flip Flop	81	0	607200	0.01
Register as Latch	0	0	607200	0.00
F7 Muxes	0	0	151800	0.00
F8 Muxes	0	0	75900	0.00

Figure.12 SAD_ARCH_1

Ref Name	Used	Functional Category
IBUF	130	IO
LUT4	82	LUT
LUT3	81	LUT
FDRE	81	Flop & Latch
LUT2	75	LUT
LUT6	41	LUT
CARRY4	24	CarryLogic
LUT5	22	LUT
OBUF	16	IO
LUT1	1	LUT
BUFG	1	Clock

Figure.13 Power Report

ADVANTAGES

1. **Reduced Processing Time:** By leveraging efficient adder compressors, the project accelerates the computation of SAD values, leading to a reduction in processing time. This decrease in processing time is crucial for real-time applications that require immediate feedback or response, such as video streaming, surveillance systems, and interactive multimedia.

2. **Enhanced Frame Rate:** Optimizing the SAD calculation using adder compressors allows for faster processing of video frames, resulting in an improved frame rate. Higher frame rates contribute to smoother and more fluid video playback, enhancing the viewing experience in real-time applications like live broadcasting, video conferencing, and gaming.

3. **Improved Motion Estimation Accuracy:** Real-time motion estimation tasks, such as object tracking and scene analysis, benefit from the project's implementation of SAD architecture with adder compressors. The enhanced speed and efficiency enable more accurate and timely detection of motion, ensuring better tracking and analysis of dynamic scenes.

4. **Responsive Feedback Systems:** Systems requiring real-time feedback to user inputs, such as interactive multimedia applications and virtual reality environments, benefit from the project's implementation. The optimized SAD architecture with adder compressors ensures prompt processing of input data, leading to more responsive and immersive user experiences.

5. **Optimized Resource Utilization**: By implementing efficient adder compressors for SAD calculation, the project maximizes resource utilization while minimizing computational overhead. This optimization is particularly advantageous for resource-constrained platforms, such as embedded systems and mobile devices, where real-time performance is critical.

APPLICATIONS

1. **Video Compression and Encoding:** In real-time video compression and encoding systems, the efficient calculation of SAD plays a vital role in motion estimation and prediction.

2. **Surveillance and Security Systems**: Real-time surveillance and security systems rely on timely analysis of video feeds to detect and respond to security threats.

3. **Object Tracking and Recognition:** In applications involving real-time object tracking and recognition, such as augmented reality (AR), robotics, and autonomous vehicles.

4. **Medical Imaging and Analysis:** Real-time medical imaging and analysis applications, including ultrasound imaging, MRI scans, and pathology diagnostics, benefit from the project's efficient SAD computation architecture..

5. **Gesture Recognition and Human-Computer Interaction:** The project's implementation of optimized SAD architecture facilitates real-time gesture recognition and human-computer interaction (HCI) in interactive multimedia systems and gaming platforms.

CONCLUSION

In conclusion, the comparison of four architectures of 8:2 adder compressors reveals significant insights into their performance metrics, including power consumption, area utilization, and delay. Among the evaluated architectures, the implementation utilizing three 4:2 adder compressors emerge as the optimal choice, demonstrating superior performance across these key criteria.

The comparison was conducted using reports generated from Xilinx, ensuring comprehensive evaluation under different technological contexts. Additionally, the effectiveness of adder compressors in calculating the Sum of Absolute Difference (SAD).

Notably, the 8:2 adder compressor constructed using the 4:2 adder compressor exhibits superior power efficiency and reduced delay compared to alternative architectures. This finding underscores the importance of selecting appropriate adder compressor configurations to optimize performance in real-time applications requiring efficient SAD calculations.

FUTURE SCOPE

1. **Optimization for Advanced Technologies:** As semiconductor technology continues to advance, future iterations of the project can explore the optimization of adder compressor architectures for cutting-edge technologies such as smaller process nodes, 3D integration, and emerging materials. This optimization would enhance performance, reduce power consumption, and enable compatibility with the latest hardware platforms.
2. **Exploration of Novel Architectures:** The project can delve into the exploration of novel adder compressor architectures beyond the scope of the current study. This includes investigating alternative configurations, innovative design methodologies, and novel circuit topologies to further improve efficiency, scalability, and versatility in real-time applications.

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Vol 19, Issue 1, 2025

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