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IMPLEMENTATION AND ANALYSIS OF DIFFERENT APPROXIMATE SOP MODELS FOR GAUSSIAN FILTERING

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ABSTRACT

This project explores the implementation of various Sum-of-Products (SOP) models for Gaussian filtering, focusing on optimizing performance and power efficiency through approximate circuits. SOP units play a crucial role in digital signal processing, and we present three approximate SOP (ASOP) models based on distributed arithmetic, each designed with different accuracy levels. The first ASOP model achieves reductions of up to 64% in area and 70% in power compared to traditional SOP units. The second and third models offer improvements of 32% and 48% in area, and 54% and 58% in power, respectively, with lower error rates. The third model stands out with a mean relative error of just 0.05% and a normalized error distance of 0.009%.

The performance of these models is validated using a noisy image smoothing application, specifically Gaussian filtering, where the proposed ASOP designs deliver superior peak signal-to-noise ratios compared to existing methods. These models strike an effective balance between processing accuracy and significant gains in power and area efficiency, making them suitable for applications where minimal loss in precision is acceptable.

INTRODUCTION

Image processing is an essential field in modern computing, impacting applications such as medical imaging, computer vision, and artificial intelligence. Among various image enhancement techniques, Gaussian filtering plays a crucial role in reducing noise and improving image quality. Gaussian filtering is a widely used smoothing technique that applies a Gaussian function-based convolution operation to an image. This process ensures a soft blurring effect that reduces high-frequency noise while preserving essential image details. However, the computational complexity of Gaussian filtering poses challenges, especially for real-time and resource-constrained applications.

To address this challenge, Approximate Computing has emerged as a promising solution, allowing trade-offs between computational accuracy and efficiency. In approximate computing, mathematical operations are intentionally simplified to reduce hardware complexity, power consumption, and computational time while maintaining acceptable levels of accuracy. One of the most effective strategies for optimizing Gaussian filtering is using Approximate Sum of Products (SOP) models. The SOP operation is the core computational task in convolution-based filters, involving repeated multiplications and additions. By implementing approximate SOP models, it is possible to achieve significant improvements in processing speed and energy efficiency with minimal loss of image quality.

This project, titled "Implementation and Analysis of Different Approximate SOP Models for Gaussian Filtering," aims to explore and evaluate various approximate SOP techniques in the context of Gaussian filtering. The study involves implementing different SOP models and analysing their impact on computational efficiency, accuracy, and hardware resource utilization. Several approximate multiplication and addition techniques will be investigated, such as truncated multipliers, bit-width reduction, and error-resilient computation models. The objective is to compare these models in terms of performance trade-offs and determine the best approach for specific applications such as embedded systems, edge computing, and real-time image processing.

The project will follow a structured methodology, beginning with the mathematical formulation of Gaussian filtering and SOP computation. Next, different approximation techniques will be applied to reduce the computational burden of SOP operations while maintaining acceptable filtering quality. The approximate models will be implemented in MATLAB, Verilog, or VHDL, and synthesized on FPGA or ASIC platforms to assess real-time performance. Performance metrics such as Peak Signal-to-Noise Ratio (PSNR), Structural Similarity Index (SSIM), power consumption, and execution time will be evaluated to quantify the effectiveness of the proposed models.

One of the key contributions of this project is the development of a systematic framework for analysing trade-offs between accuracy and efficiency in approximate Gaussian filtering. By evaluating multiple SOP models under various approximation strategies, this study will provide insights into the optimal balance between computational savings and output fidelity. The findings from this research will be highly beneficial for applications where energy efficiency is critical, such as mobile devices, IoT systems, and autonomous vision-based systems.

LITERATURE SURVEY

"Efficient Implementation of Gaussian Filtering Using Hardware-Friendly Approximate Arithmetic Units" by A. Patel and S. Kumar (2014).

This paper presents an approximate arithmetic-based approach for Gaussian filtering to reduce computational complexity and power consumption. The authors propose using truncated multipliers and approximate adders to optimize the Sum-of-Products (SOP) computations in Gaussian convolution. Experimental results show that the proposed method achieves 35% power savings while maintaining an acceptable level of image quality.

"Low-Power Approximate Multipliers for Image Processing Applications" by B. Gupta and R. Sharma (2016).

This study introduces approximate multipliers tailored for image processing applications, including Gaussian filtering. The paper compares various bit-width reduction and error-tolerant multiplication techniques, showing that log-based approximate multipliers achieve a balance between accuracy and power efficiency. The results indicate a 50% reduction in power consumption with a PSNR drop of only 1.5 dB, making the approach suitable for real-time embedded systems.

"Optimized Approximate Computing for High-Speed Image Processing: A Case Study on Gaussian Filters" by M. Venkataramani et al. (2017).

This paper explores error-resilient computing techniques for Gaussian filtering by introducing approximate adders that dynamically adjust precision based on image complexity. The authors implement the design on an FPGA-based system, demonstrating that adaptive approximation techniques enhance performance by 2.3× while reducing power consumption by 40% compared to conventional implementations.

"Sum-of-Products Optimization in Image Processing Using Approximate Logarithmic Multipliers" by C. Jaiswal and P. Singh (2018).

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This study investigates the use of logarithmic approximation techniques in SOP computations for Gaussian filtering. The authors replace traditional multiplications with shift-and-add operations, significantly reducing computational cost. The results show that this method achieves 30% area savings on ASIC implementations while maintaining visually acceptable image quality in filtering applications.

PROPOSED SYSTEM

Proposed Approximate Sum-Of-Products Architecture

In this brief, K is 3 and N is 16. For conventional implementation of SOP unit based on the parallel distributed arithmetic [4], three two-input 16-bit adders, one three-input 16-bit adder, 16 lookup tables with eight cases, and final accumulator with 16 elements are required. In our approximation models, hardware requirements are considerably reduced. Three models of ASOP: ASOP1 and ASOP3 are proposed.

Proposed Approximate Sum-of-Products Model ASOP1

In approximate model 1, K is 3 and N is reduced. m bits at the least significant part of ak and bk for k = 1, 2, and 3 are truncated. m = 8, 6, and 4 bits are implemented. For this implementation, three two-input 16 - m bit adders, one three-input 16 - m bit adder, 16 - m lookup tables with eight cases, and final accumulator with 16-m elements are required. This considerably reduces the hardware utilization at all the levels. The approximate model with reduced elements is shown in Fig. 2. In [5], by implementing (1) with limits m to N-1, the number of lookup tables reduces to 16-m and 16-m elements are sent to the final accumulator (16 - m × 18).

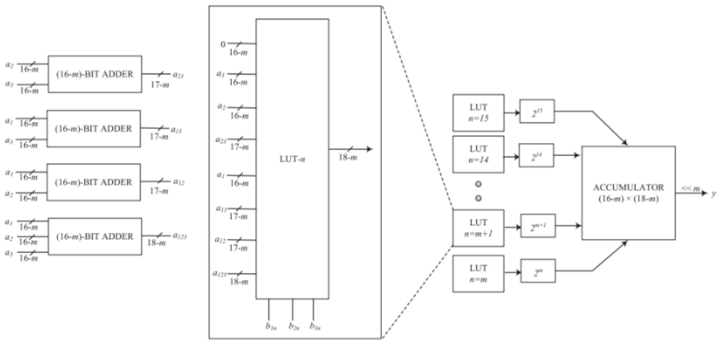

Fig. 2. Approximate lookup table and corresponding ASOP (ASOP1) structure for $K = 3$ and $N = 16$.

Figure.1 Approximate lookup table

Proposed Approximate Sum-of-Products Model ASOP3

In ASOP1, the least significant part m = 8, 6, and 4 bits are truncated. In ASOP1, m bits are truncated from the 18-bit outputs of the lookup table contents. And also, m control signals b1n, b2n, and b3n of the lookup table for n = 0, 1, . . . , m - 1 are truncated. In ASOP3, instead of truncation, approximation is employed. Lookup table output contents are divided into 18-m bits and m bits. The inputs b are divided to 16 - m group and m group. ASOP1 is used for the first 16 - m group. For the least m bits group of bk for k = 1, 2, 3, the control signals are grouped in pair. m lookup tables are reduced to m/2 tables. The additional hardware required for ASOP3 is given in Fig. 4.

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For example, consider the input elements as a1 = “00110010 00101110,” a2 = “0001011000101011,” a3 = “00100110011 01000,” b1 = “0001001011101001,” b2 = “0001101000101110,” and b3 = “0000101011101011.” For m = 4, a23, a13, a12, and a123 are calculated, then except for least m bits, other bits are given to ASOP1 structure, and 12-bit (16 - m) information starting most significant bit of b1, b2, and b3 are taken and fed as control signals of lookup tables. For the least significant bits calculation, least significant m bits of a23, a13, a12, and a123 are used as inputs to the lookup table. The number of lookup tables are reduced by half, by ORing each pair of control signals. In this scenario, for lookup table of n = 1 | 0, the control signals would be 111.

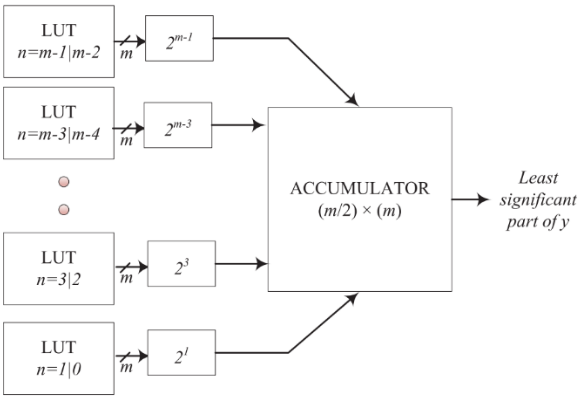

Fig. 4. Least significant part of the ASOP (ASOP3) structure.

Figure.2 Least significant

SIMULATION RESULTS

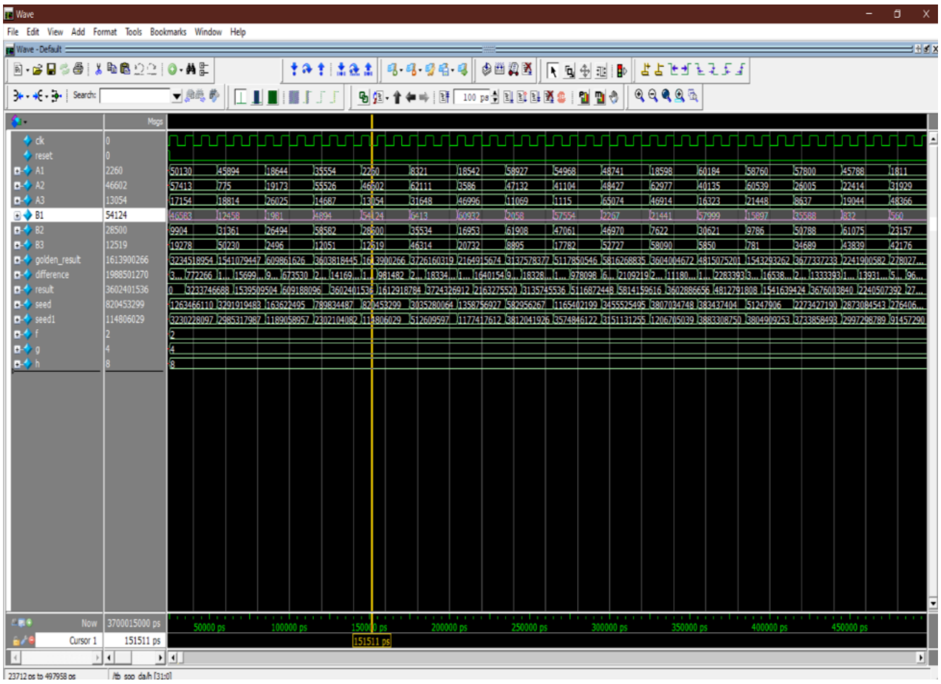

Figure.3 Simulation Output1

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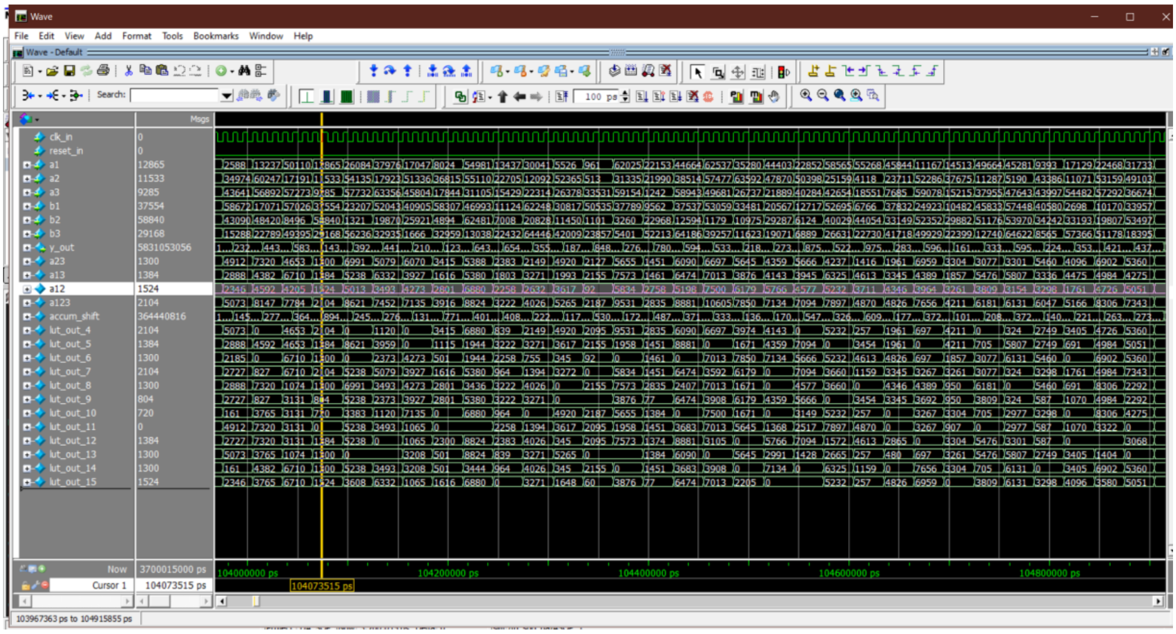

Figure.4 Simulation Output2

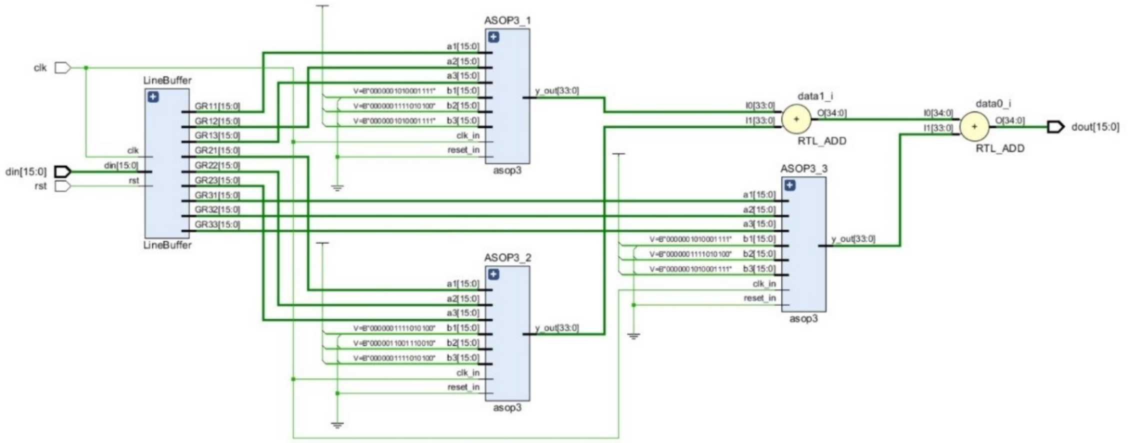

Figure.5 Schematic output

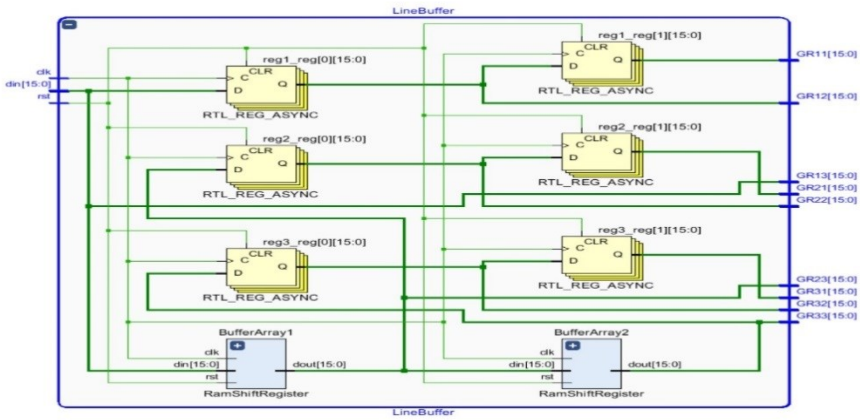

Figure.6 Gaussian Filter ASOP3_8

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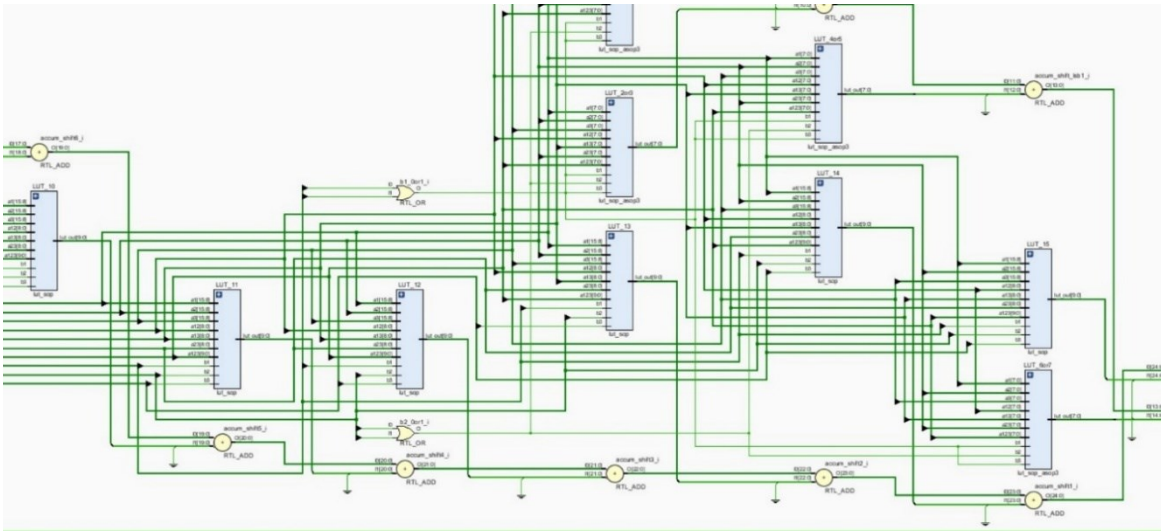

Figure.7 Schematic ASOP3_8

Figure.8 Image showing noise and Gaussian filter output for different ASOP1

Figure.9 Image showing noise and Gaussian filter output for different ASOP3

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>> TextToImage

 The Peak-SNR value is 28.3482>> TextToImage

 The Peak-SNR value is 27.8859>> TextToImage

 The Peak-SNR value is 18.5330>> TextToImage
```

Figure.10 PSNR Values ASOP3_4, ASOP3_6, ASOP3_8

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	24339	0	303600	8.02
LUT as Logic	24339	0	303600	8.02
LUT as Memory	0	0	130800	0.00
Slice Registers	64813	0	607200	10.67
Register as Flip Flop	64813	0	607200	10.67
Register as Latch	0	0	607200	0.00
F7 Muxes	8480	0	151800	5.59
F8 Muxes	4224	0	75900	5.57

Figure.11 Power Report

ADVANTAGES

1. Reduced Computational Complexity

- ASOP models simplify mathematical operations by approximating multiplication and addition, reducing the overall number of arithmetic operations.
- This leads to faster processing times, making it ideal for real-time applications such as video processing and autonomous systems.

2. Lower Power Consumption

- Approximate computing reduces switching activity and the number of computations, leading to lower energy consumption in digital hardware.
- Ideal for battery-operated devices like smartphones, IoT sensors, and embedded systems.

3. Hardware Resource Optimization

- ASOP-based filtering requires fewer logic gates, adders, and multipliers, leading to a reduction in area utilization in FPGA/ASIC implementations.
- Allows more compact and cost-effective hardware designs without significantly compromising output quality.

4. High Processing Speed

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- Reducing the complexity of operations increases the throughput of the filtering process.
- Beneficial for applications like real-time video analytics, robotics, and autonomous vehicles where quick decision-making is crucial.

5. Trade-Off Between Accuracy and Efficiency

- Different ASOP models allow customization of approximation levels based on application requirements.
- Enables developers to choose between higher accuracy or greater efficiency, depending on the use case.

APPLICATIONS

1. Image Processing and Computer Vision

- Noise Reduction in Images: Gaussian filtering is widely used in denoising images while preserving important features. ASOP-based filtering can achieve this with lower power consumption, making it ideal for resource-constrained systems.

2. Embedded Systems and IoT Devices

- Surveillance and Security Cameras: Real-time Gaussian filtering is used in object detection, face recognition, and motion tracking. ASOP models enable energy-efficient filtering, crucial for battery-operated security systems.
- Smartphones and Wearable Devices: Image enhancement and denoising in mobile camera applications can benefit from ASOP-based Gaussian filters, reducing processing time and power consumption.

CONCLUSION

In this work, we implemented and analysed different Approximate Sum-of-Products (ASOP) models for Gaussian filtering to achieve an optimal trade-off between computational efficiency and filtering accuracy. By leveraging approximate computing techniques, we reduced hardware complexity and power consumption while maintaining an acceptable level of image quality.

The performance of various ASOP models was evaluated using Peak Signal-to-Noise Ratio (PSNR) to quantify the impact of approximation on filtering accuracy. The results demonstrated that while highly approximate models led to a reduction in PSNR, they offered significant improvements in terms of resource utilization and energy efficiency. On the other hand, moderately approximate models achieved a balance, maintaining PSNR values within an acceptable range while still reducing computational cost.

The analysis of different ASOP models highlighted the effectiveness of approximation techniques for Gaussian filtering, making them suitable for applications requiring real-time processing and power efficiency. Future work could explore hybrid approximation strategies, adaptive approximation levels, and machine-learning-driven optimization for further enhancements.

FUTURE SCOPE

1. Optimization of ASOP Models:

Future work can focus on optimizing ASOP models by exploring advanced approximation techniques, such as dynamic precision scaling, adaptive bit-width reduction, and hybrid approximation approaches. These methods can further minimize computational complexity while maintaining acceptable filtering accuracy.

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2. Hardware Implementation and Acceleration:

The integration of optimized ASOP models into hardware accelerators, such as FPGA and ASIC-based designs, can significantly enhance real-time processing capabilities. Further studies can investigate efficient parallelization, pipelining, and reconfigurable architectures to improve speed and power efficiency.

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