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Energy Efficient Compact Approximate Multiplier for Error Resilient Applications

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Abstract –

The primary goal of approximate computing is enhancing system performance, such as energy efficiency, speed, and form factor. Despite the growing use of approximate multipliers, the design of efficient approximate compressors a fundamental multiplier block remains a significant challenge. In this brief, 8-transistor and 14-transistor 4:2 compressors are proposed. Both compressors exploit CMOS technology and a constant and conditional approximation of selected inputs, exhibiting fewer negative errors. As a result, a resource-expensive error recovery module is eliminated, yielding superior performance as compared with prior art. The 14-transistor architecture yields a lower error rate compared to the 8-transistor architecture, trading off lower area for higher accuracy. The compressor- tailored circuit architecture is also proposed and evaluated using image multiplication. The proposed multiplier exhibits 50% area savings and 93% lower power-delay-product compared to the exact multiplier, as well as higher accuracy, and 38% PDP enhancement compared with the state-of-the-art.

Keywords – Approximate computing, compressor, multiplier, image multiplication.

I. INTRODUCTION

Improving energy efficiency, reducing power and decreasing path delay are the main challenges in modern digital system design. There exist several applications in multimedia and machine learning which do not require accurate results. These applications are able to tolerate inaccuracies and hence one may use approximate computing to significantly reduce design costs of arithmetic circuits and achieve improvements in cell area, power consumption and path delay metrics. Multiplication is an arithmetic operation used in digital processors employed to handle applications like Image processing. In the authors propose several approximate 4 × 4 multiplier designs, using 4:2 compressors which are then extended to larger 8 × 8 multiplier designs. In this article we design 4 × 4 multipliers using 4:2 compressors and the technique of, encoded sum of partial products. We then propose the use

of an approximate 3-bit adder to calculate the sum of partial products obtained from the 4 ×4 multipliers in less significant bit positions in order to construct larger 8×8 multipliers. As a convention we denote the multipliers proposed. This exposes to us the improvements that can be achieved in cell area, power and delay using this technique of approximate computing. Multiplication is one of the simple functions which are used in digital signal processing applications (DSP). Multipliers require more hardware resources and processing time compared to that of adders. In order to achieve the high speed and low power demand, the various multipliers has to design to meet requirements of current VLSI industry requirements. Multipliers are not only used in processor, but also used in other part of processor designs such as various data units. In general, two numbers such as multiplier and multiplicand are multiplied and generate a product value. All multipliers architectures are built with basic blocks such as Half Adders (HA), Full Adders (FA), and various complex adder.

II. Modified approximate 4:2 compressor

The exact 4:2 compressor uses two full adders connected approximately. To reduce hardware cost coupled with the fact that an XOR gate is slower and less energy efficient compared to the AND and OR gates, we employ only AND and OR gates as proposed in while designing the approximate 4:2 compressor. To overcome this the input signals to the compressor are encoded using propagate and generate signals. In, two approximate 4:2 compressors are proposed, prioritizing circuit efficiency over accuracy with reduced delay. The multiplier in exhibits higher error rates and increased area. An approximate compressor in computes error distances (ED) using a hash table and mitigates errors with an error recovery module (ERM), yielding high accuracy and area consumption. In a configurable multiplier with exact and approximate modes is proposed, exhibiting high area and up to a 50% output errors. Majority logic (ML) and CMOS-based circuits significantly reduce area and power consumption at the expense of a higher error rate. Circuit-stacking-based approximate com- pressors, algorithm-based optimization with error control modules, and probability-based error correction techniques show reduced error while requiring a larger area.

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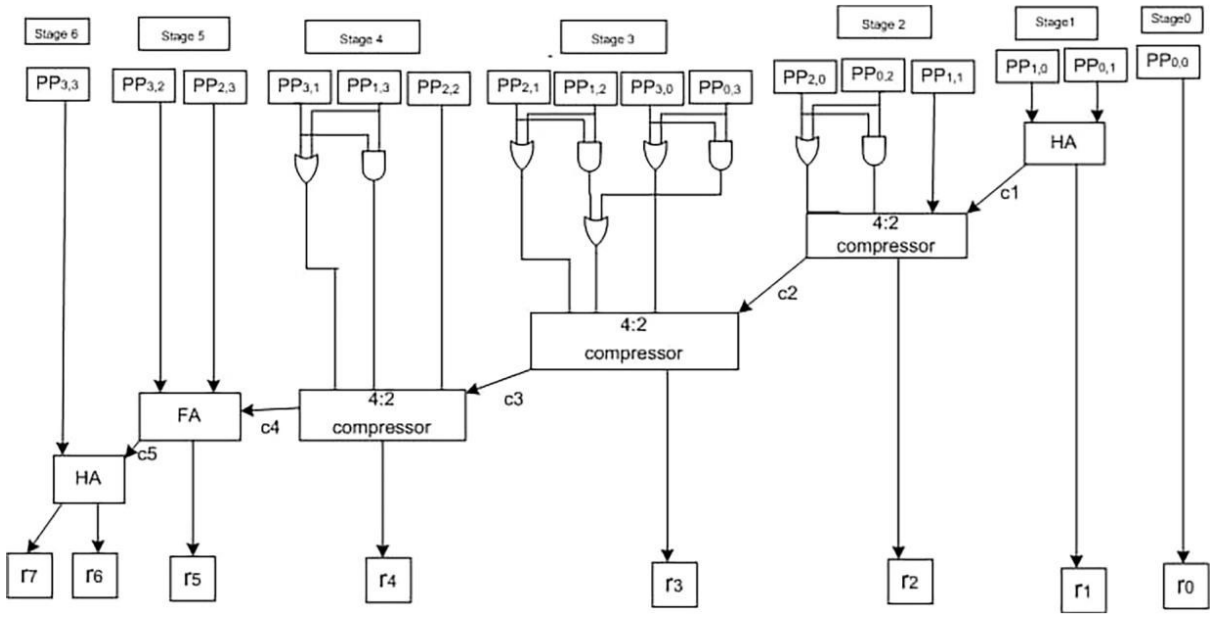

Fig.1. Approximate 4:2 compressor

After designing the multipliers we want to evaluate their accuracy i.e. the obtained result vs the actual result. We first use the mean relative error distance (MRED) to quantify the accuracy of the approximate multiplier designs. To compute the MRED we first calculate the error distance (ED) given by, $ED = |M'-M|$ where M' refers to result produced by the approximate multiplier while M represents the exact result. We then compute the relative error distance (RED) given by,

$$RED = ED/M$$

Which is the ED divided by the exact result M for every input combination. The average value of RED's over all possible input combinations is the MRED.

III. PROPOSED METHOD

Majority logic (ML), a robust and fault-tolerant digital logic design paradigm, leverages the power of collective decision making to enhance reliability, simplicity, and efficiency in electronic circuits. An ML gate functions through an odd input logic principle, generating a True (False) output when more than half of its inputs are True (False). Due to the increased configurability, ML-based circuits typically require fewer gates. Hence, the design of ML-based compressors is a promising approach for reducing the circuit area without sacrificing accuracy. Fig. 2 shows our design flow for an 8- bit multiplier to produce a combination of fixed, approximate, and exact outputs. The ML-based approximate components (c.f., Section III-A and III-B) generate the approximated bits and transfer them to

the simplified circuits consisting of half adder (HA) and full adders (FAs) with at least one fixed input.

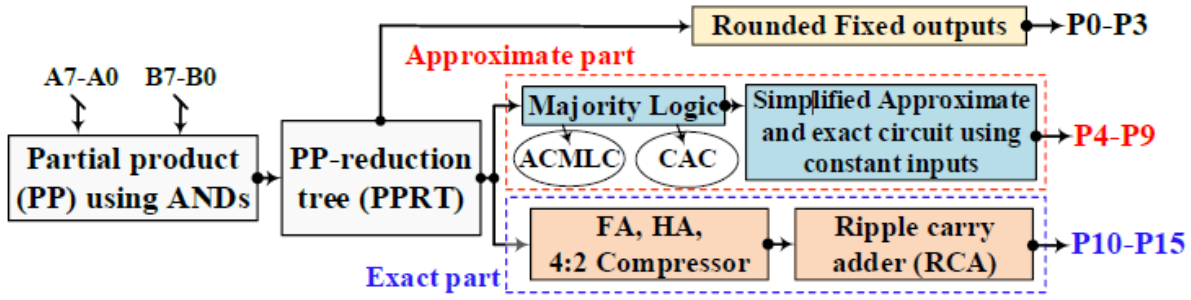

Fig.2. Proposed design flow of 8-bit multiplier.

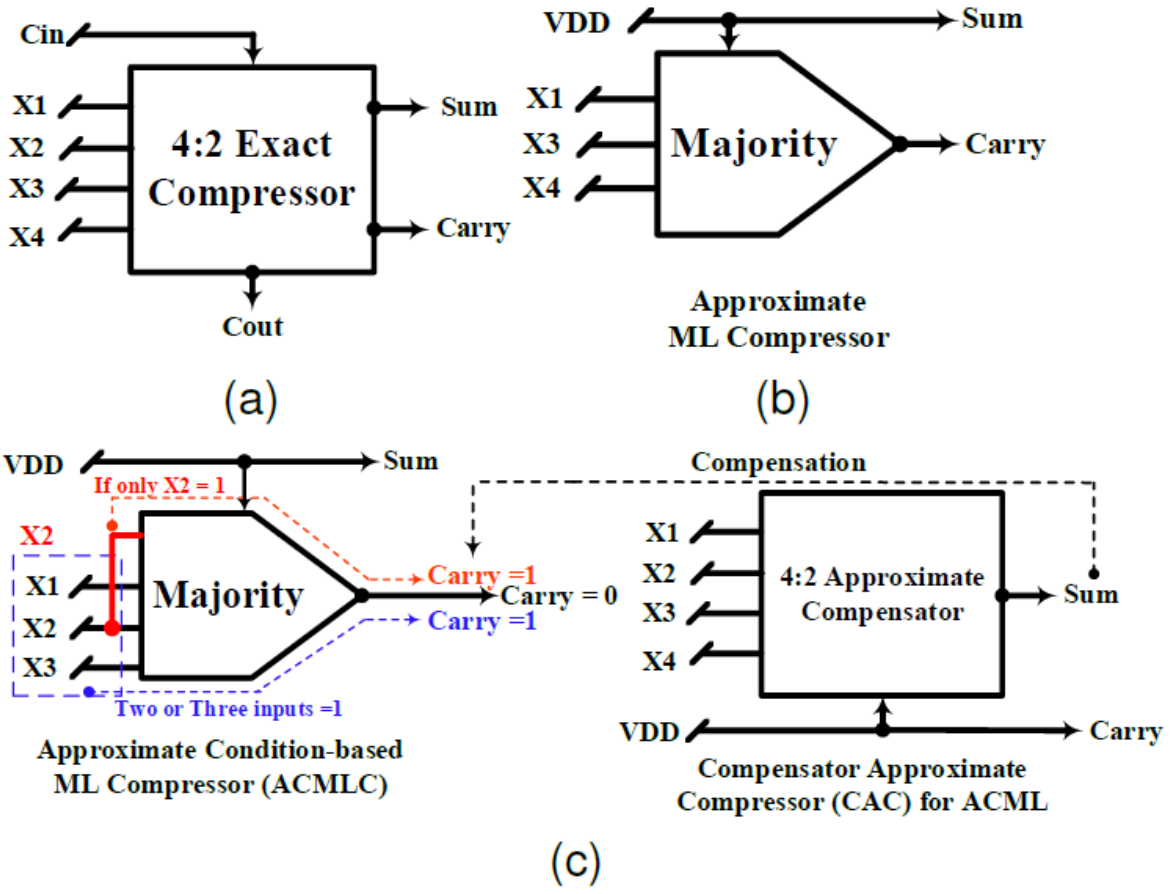

Fig.3. Schematics of the compressor circuits (a): Exact. (b): ML-based, and (c): ACMLC and CAC, respectively.

The ML circuit architecture described is utilized and improved with a two-stage approximation approach. Fig. 3 shows the circuit schematics, including the cell view of the exact compressor circuit (c.f., Fig. 3a), ML-based compressor (c.f., Fig. 3b), and the proposed approximate condition based ML (ACMLC) compressor and compensator approximate

compressor (CAC) for the ACMLC (c.f., Fig. 3c). Note that the ML-based compressor considers only three out of four inputs (input X2 is ignored) and a fixed output (Sum = VDD). The Carry output is True if at least two of the inputs are '1' (i.e., X1 + X3 + X4 equals two or three), yielding a total of four negative and four positive errors. Extensive research has recently been conducted on the impact of negative and positive errors in approximate circuits. In the approximate region of a multiplier, each approximate compressor generates an error, leading to a significant error distance in the columns. Employing an error recovery module (ERM) based on specific input patterns for individual approximate compressors is crucial for minimizing overall error distance and reducing negative errors. Consequently, the importance of ERM circuits for mitigation of negative errors has been emphasized. Employing a multiplier that utilizes approximate compressors intelligently, owing to their low negative error rates and consistent error generation, eliminates the necessity for ERM. Accordingly, we propose the ACMLC circuit architecture, as shown in Fig. 3c, to simultaneously mitigate negative error and reduce the circuit area. In addition to the typical majority based approximation (i.e., one of three inputs, X4, is ignored and Sum is set to VDD), the Carry output is '1' in the following two scenarios: (i) two or three of the inputs are '1' (similar to [7]) as highlighted in blue in Fig. 3c, or (ii), only X2 is '1' (and the rest of the inputs are '0'), as highlighted in red in Fig. 3c. For all other input combinations, the Carry output is '0', yielding Sum ACMLC = VDD, Carry ACMLC = (X1 · X3) + X2. Compressor architectures that exhibit a higher number of negative errors, a compensator circuit is needed to enable the data flow between the approximate and exact sub-circuits of a multiplier. To address this challenge, we propose CAC circuit architecture (c.f., Fig. 3c) for ACMLC compensation. The architecture is based on a typical 4:2 compressor architecture with a fixed carry output, Carry = VDD and approximate Sum, Sum = (X1 · X2)(X3 + X4) + (X3 · X4). With this approach, there are only seven errors (all with error distance of ED = 1), and one negative error. Alternatively, the number of transistors is increased from eight in ACMLC to 14 in CAC. The simplicity of the proposed ACMLC compressor as compared to the ML-based compressor and CAC naturally leads to lower area. We show the schematic of the proposed multiplier in Fig. 4 leveraging the proposed ACMLC-based compressor and CAC. Our proposed approximate multiplier comprises three components, truncation, constant truncation, approximation, and exact compute, each contributing to the computation of partial products (PPs) in Stage 1 (c.f., Fig. 4). One of the common methods in these circuits is to truncate at least four LSB columns of PPs (for an 8-bit multiplier). This approach is Best and

worst results are highlighted in green and red, respectively. effective with highly accurate approximate components. To mitigate a higher number of errors with the proposed compressors, an alternative method is preferred in this work based. In constant values are assigned to several LSB PP bits. The probabilities of generating 0 or 1 for each of the circuits generating p0, p1, p2, p3, and p4 were investigated by applying different inputs. As per observations, the rightmost four LSB bits are fixed at p0p1p2p3=0110. By fixing the LSB bits to a constant value, the number of required gates is reduced. In this case, ten AND gates are removed from the first four columns of the proposed multiplier circuit (as shown with the gray triangular shaded area in Fig. 4).

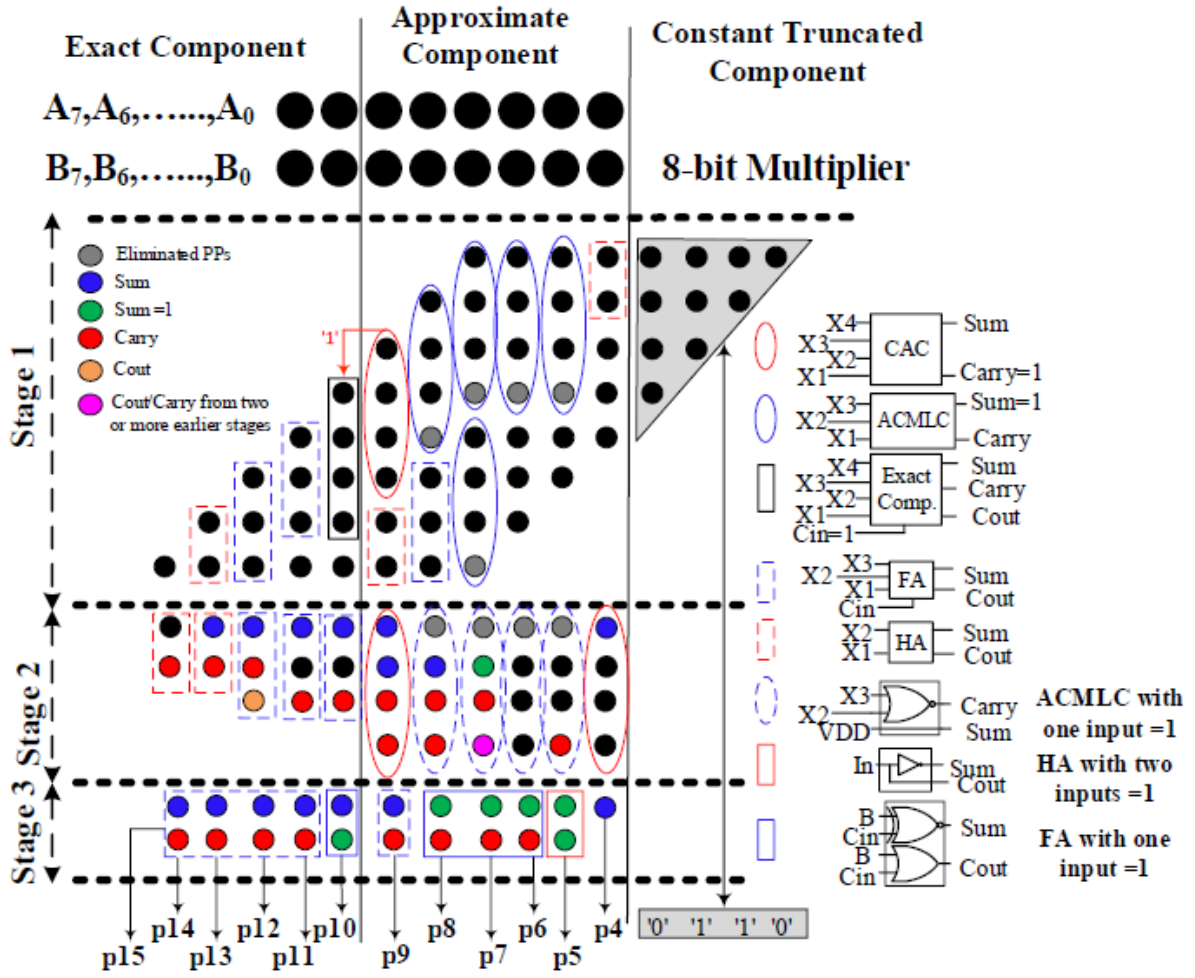

Fig. 4. Proposed multiplier schematic using the proposed ACMLC-based compressor and CAC.

The approximate component of the proposed multiplier comprises five ACMLC-based compressors, a CAC, two exact HAs and an exact FA. With the proposed 3-input ACMLC based compressor, one of the four PPs is effectively eliminated, resulting in the

elimination of five AND gates within a single PP stage. The eight unused (solid black circles) AND gates in that stage are repurposed in the second stage to form a compressor-based chain, thereby reducing the overall area. The proposed CAC is used in the last column of the approximate component to transfer Carry = 1 to the exact component, simplifying the exact compressor circuit. Finally, the simplified exact compressor (with constant input, Cin = 1) is only utilized once in the entire multiplier. Note that the use of the exact HAs and FA enhances multiplier accuracy, complementing the small area of the proposed ACMLC-based compressor and CAC.

IV. RESULT

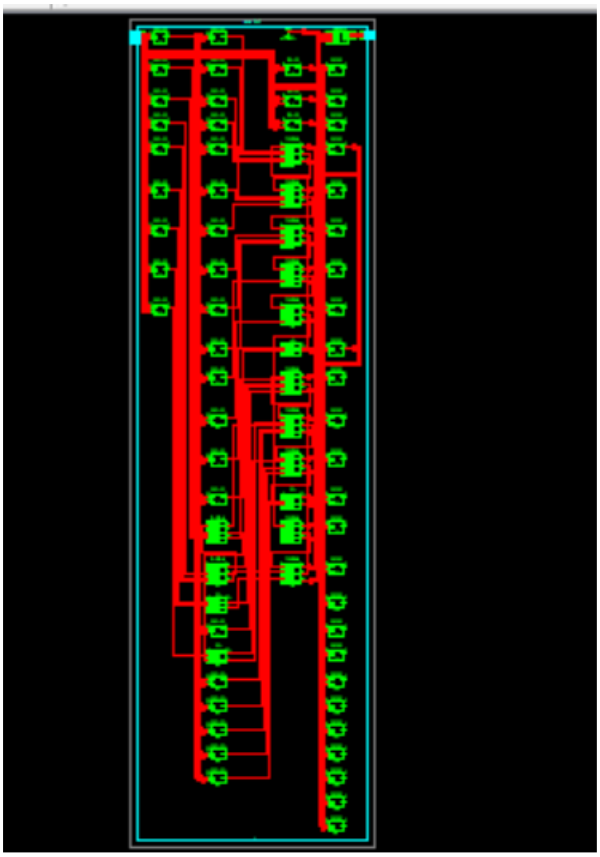

FIG:5. RTL SCHEMATIC FOR PROPOSED APPROXIMATION MULTIPLER

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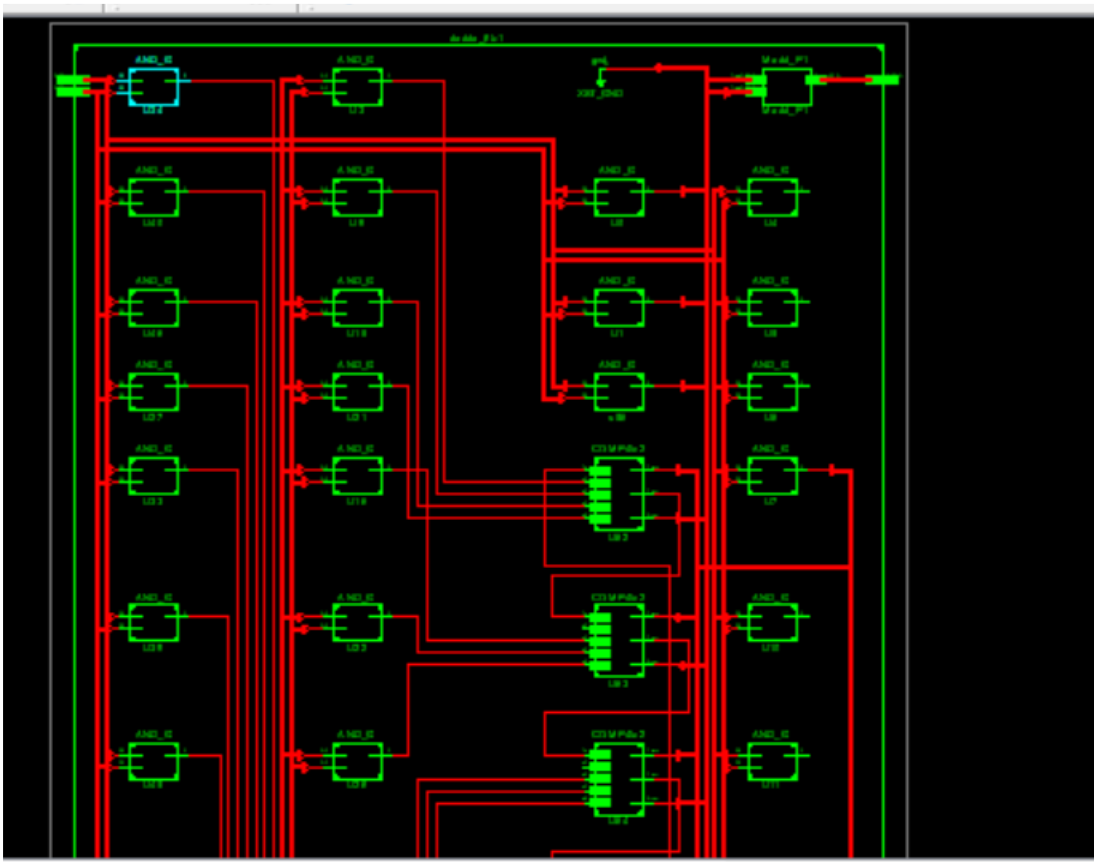

Fig:6. RTL schematic for existing Multiplier

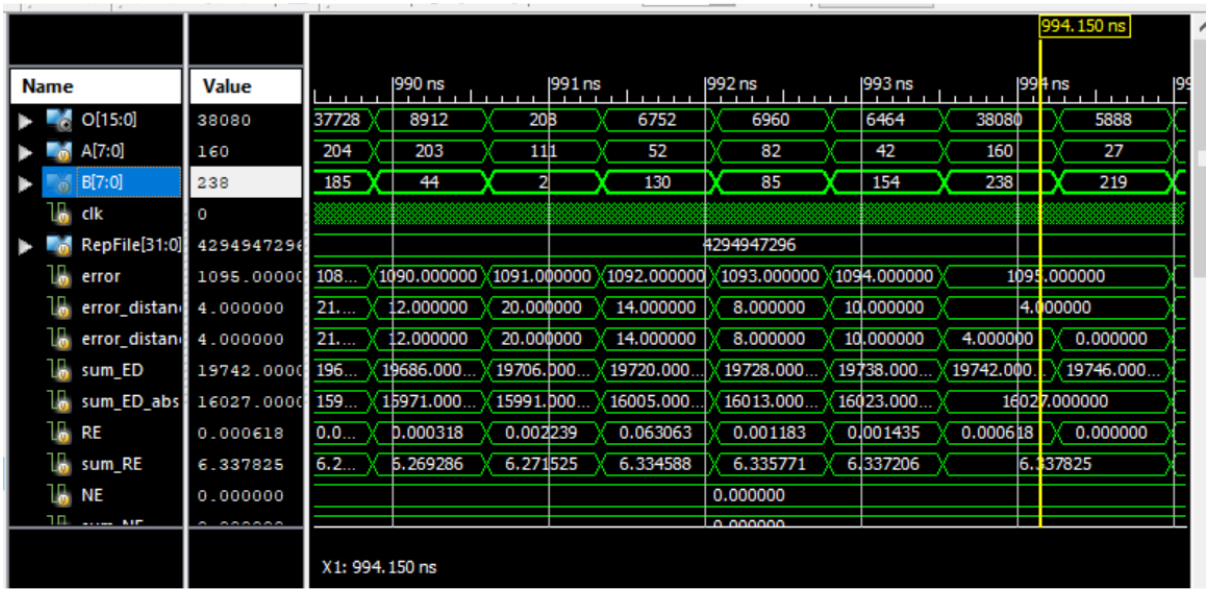

Fig:7. Output Results for Approximation multiplier

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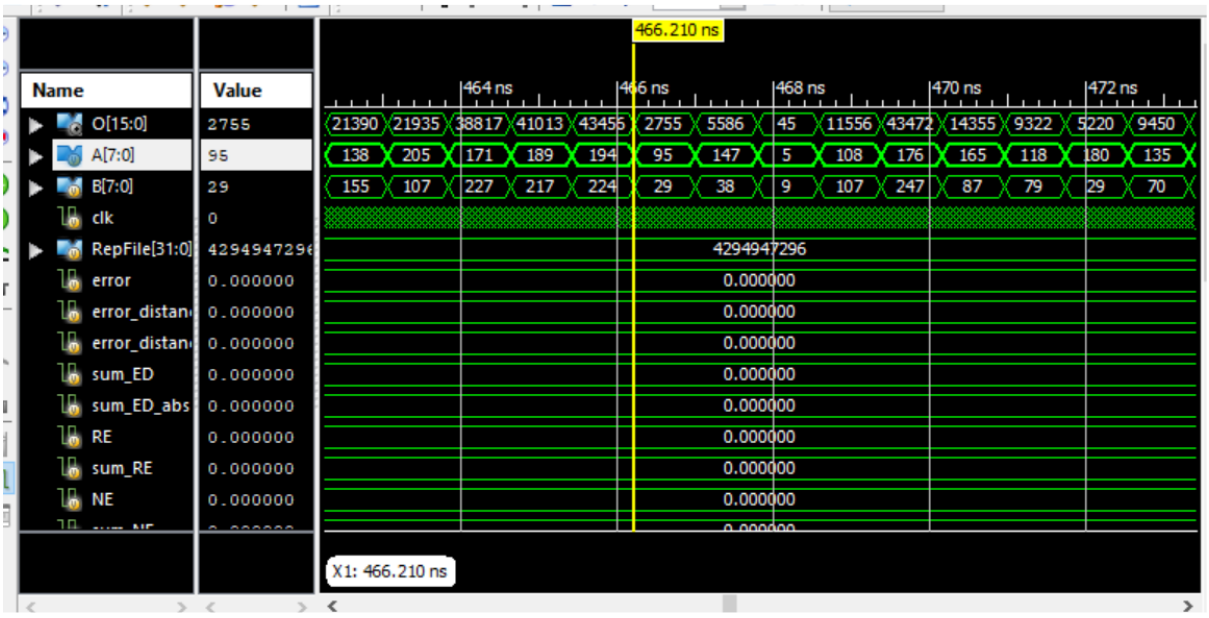

Fig:8. Output Results for Exact multiplier Existing system

Multiplication is crucial in image processing tasks, demanding high computational resources. Therefore, efficient approximate multipliers are crucial for effective and faster computation with acceptable precision. To evaluate the performance accuracy, we evaluated our multiplier using image multiplication in MATLAB. The quality of image multiplication remains consistent across all evaluated circuits, as evidenced by the PSNR values, ranging between 39.54 dB and 40.63 dB. The OA metric is computed as (TP+TN)/(total number of samples), where TP and TN are, respectively, the true positives and true negatives, and are computed in MATLAB. While the OA for the proposed circuit is comparable to the OA of state-of-the-art approximate multipliers, the FoM for the proposed solution is significantly higher than prior art, exhibiting higher accuracy per unit energy. Note that the proposed circuit yields 91% OA with a 13% and 39% higher FoM than the second and third best solutions. Lower values of FoM1 and FoM2 and higher values of FoM3 and FoM4 indicate better performance of multipliers. Due to the excellent power and area characteristics shown by the PDP and PDAP metrics and considering the typical multiplication quality determined by the NMED metric, our multiplier demonstrates superior performance across all four FoMs.

CONCLUSION

In this brief, we proposed an 8-transistor ACMLC compressor, a 14-transistor CAC, and an approximate 8-bit multiplier for accurate and efficient image multiplication. The compressor has small footprint and low power consumption at the expense of a relatively

high error rate. To compensate for the negative errors, we propose CAC, exhibiting seven errors, with only one being negative. We propose an ACMLC/CAC-based approximate multiplier to exploit the proposed compressors' unique characteristics. Relative to an exact multiplier, the proposed multiplier exhibits 50% area reduction and 93% power savings. The proposed multiplier exhibits superior performance across most evaluated metrics compared to state- of-the-art approximate multipliers. The Pareto results reveal that despite their lower accuracy, ML-based proposed circuits are promising for low-power and energy dissipation applications.

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