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OPTIMIZED VLSI ARCHITECTURE FOR APPROXIMATE MULTIPLIER WITH REDUCED AREA AND POWER

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Abstract: Approximate computing can decrease the design complexity with an increase in performance of area, delay and power efficiency for error resilient applications. This brief deals with a new design approach for approximation of multipliers. Approximate computing can decrease the design complexity with an increase in performance of area, delay and power efficiency for error resilient applications. This brief proposes a novel 4-2 approximate compressor which is complementary with other compressors from earlier work and constructs a approximate multiplier using brent kung adder based on the compressors. According to the simulation results, the proposed approximate multiplier has good performance. The implementation, synthesis and simulation is executed and noted in the Xilinx-vivado in verilog hdl language.

Key words: Approximation algorithm , Exact and approximate Compressors

I. INTRODUCTION

Multipliers assume a urgent part in these day's virtual sign handling and different projects. With progresses in age, numerous specialists have endeavored and are trying to format multipliers which give both of the accompanying plan targets – unnecessary speed, low power utilization, routineness of design and thus less area or even blend of them in a solitary multiplier along these lines making them reasonable for assorted high speed, low strength and smaller VLSI execution. Media processing applications, such as image processing and machine learning, have developed rapidly over the past two decades. For these applications which involve human perception, approximate computing is an effective way to improve power efficiency [1]. Approximate multipliers are the most popularly used arithmetic units and are easily modifiable. The three parts of a multiplier that approximation methods could be applied to are partial product creation, partial product accumulation and reduction, and final addition. The second part reducing partial products by accumulation consumes the most resources during the multiplication process [2]. Approximate compressors such as 4-2 compressors are usually used to accelerate the accumulation. Kong and Li [3] broadly classify compressors into high-accuracy and lowaccuracy categories based on the number of output errors. Low-accuracy approximate compressors mainly focus on reducing power dissipation. Momeni et al. [4] proposed a symmetrical approximate 4-2 compressor, but it produces a plus-one error when all four inputs are 0, which is the most common case for all input patterns. Sabetzadeh et al. [5] proposed a simple compressor only consists of a majority gate and assumes

S output is a constant 1. This brief studies approximate compressors and shows the following contributions:

• A new tiny area approximate 4-2 compressor with only four logic gates is proposed. The compressor's output errors occur regularly with specific input patterns.

• Esposito's compressors are combined in a novel way to adjust the error probability that different input patterns will occur. The combination reduces error and significantly enhances electrical performance.

• An approximate multiplier with low resource cost is developed based on the proposed compressor. The simulation results demonstrate that the proposed approximate multiplier outperforms the present multipliers in terms of PDAP and accuracy tradeoff.

II. LITERATURE SURVEY

A.G. M. Strollo, E. Napoli, D. De Caro, N. Petra, and G. D. Meo, "Comparison and extension of approximate 4-2 compressors for lowpower approximate multipliers," Recursive multipliers (RMs) have been classified as a class of low-power multipliers because they provide a wide-range of power-quality configuration options. 2×2 multipliers are the constitutional building blocks of this recursive topology; however, most of the state-of-the-art approximate recursive designs are based on a 4×4 building blocks. Therefore, the design space exploration of AxRMs using 2×2 multipliers is still an open-research problem.

To add the configurability and flexibility in the design of AxRMs such 2-bit multipliers are required that exhibit high-performance and low-area. In this article, two approximate 2×2 multipliers are proposed that exhibit double-sided error distribution feature. Compared to the existing best-approximated 2×2 multiplier, the proposed design achieves a reduction of 52 percent in area and exhibits an improvement of 25 percent in terms of delay while having a bounded error behavior. Then, three 8×8 multipliers of variable accuracy are designed using different configurations of approximate 2×2 multiplier.

AxRM1 is the most-accurate design; an improvement of 50 percent in terms of mean relative error distance (MRED) is achieved compared to the existing best MRED-optimized design. AxRM3 has similar MRED compared to the previous best 2×2-based AxRM (called MACISH); however, AxRM3 exhibits 13 percent better PDP than MACISH due to the use of low-power and high-performance 2×2 multipliers in building larger multipliers. The proposed approximate multipliers are applied to cutting-edge error-tolerant application, i.e., convolutional neural networks. AxRM2 provides the best quality-power trade-off, 32.64 percent power savings are achieved with 1.10 percent better classification accuracy.

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Vol 19, Issue 2, 2025

III. APPROXIMATE MULTIPLIER USING BRENT KUNG ADDER

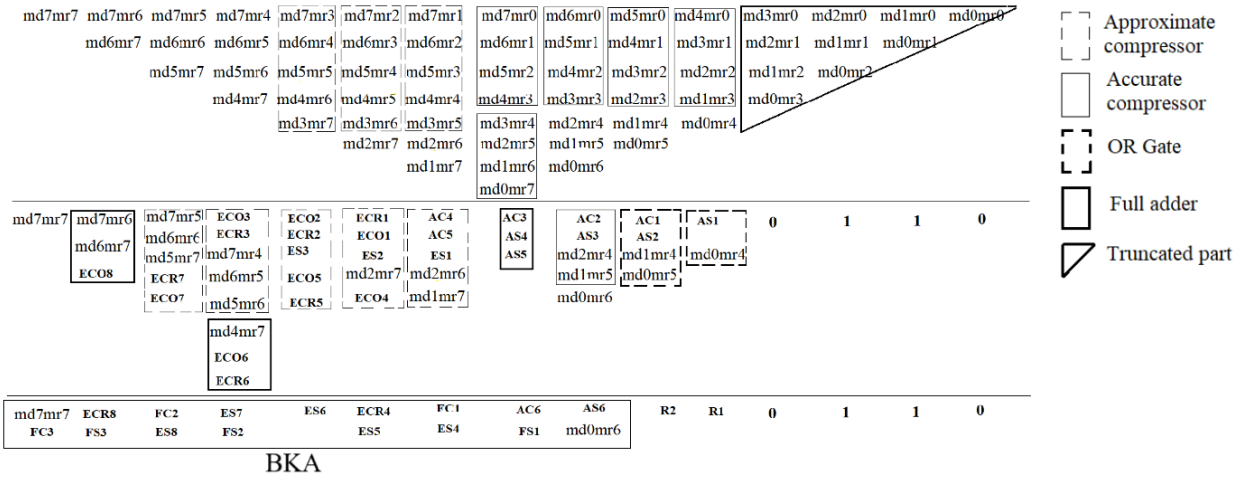

Fig. 1. proposed approximate multiplier structure

Approximate multipliers are widely being advocated for energy-efficient computing in applications that exhibit an inherent tolerance to inaccuracy. However, the inclusion of accuracy as a key design parameter, besides the performance, area and power, makes the identification of the most suitable approximate multiplier quite challenging. In this paper, we identify three major decision making factors for the selection of an approximate multipliers circuit: (1) the type of approximate area efficient compressor and dual quality compressor used to construct the multiplier, the architecture, i.e., array or tree, of the multiplier and the placement of sub-modules of approximate and exact multipliers in the main multiplier module. Based on these factors, we explored the design space for circuit level implementations of approximate multipliers. We used circuit level implementations of some of the most widely used compressors.

EXACT 4:2 COMPRESSOR

The general block diagram of an exact 4 : 2 compressor is shown in Figure 1. It comprises of five inputs, three outputs and two cascaded full adders. A1, A2, A3, A4 and CIN are the inputs and COUT, CARRY and SUM are the outputs of the exact 4:2 compressor. COUT, CARRY and SUM are given as

$$COUT = A3(A1 \oplus A2) + A1(A1 \oplus A2) \quad (1)$$

$$CARRY = CIN\ (A1 \oplus A2 \oplus A3 \oplus A4) + A4(A1 \oplus A2 \oplus A3 \oplus A4) \quad (2)$$

$$SUM = CIN \oplus A1 \oplus A2 \oplus A3 \oplus A4 \quad (3)$$

A compressor chain is shown in Figure 1. CIN represents the input carry from the preceding 4 : 2 compressor that has processed the lower significant bits. CARRY and COUT are the outputs of order ‘1’ with higher significance than the input CIN . Table 1 presents the truth table for the exact compressor.

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Vol 19, Issue 2, 2025

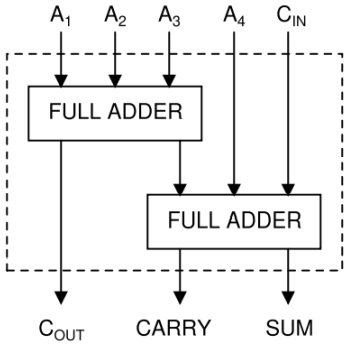

Fig2. Exact 4:2 compressor.

AREA-EFFICIENT APPROXIMATE 4 : 2 COMPRESSOR

The proposed high speed area-efficient 4 : 2 approximate compressor is shown in Figure 3. The compressor inputs are A1, A2, A3 and A4, outputs are CARRY and SUM. A multiplexer (MUX) based design approach is used to generate SUM. Output of XOR gate acts as the select line for the MUX. When select line goes high, (A3A4) is selected and when it goes low, (A3 + A4) is selected. By introducing an error with error distance 1 in the truth table of the exact compressor, the proposed 4 : 2 compressor is able to reduce carry generation logic to an OR gate. The logical expressions for realisation of SUM and CARRY are given below.

$$SUM = (A1 \oplus A2)A3A4 + (A1 \oplus A2)(A3 + A4) \quad (4)$$

$$CARRY = A1 + A2 \quad (5)$$

From the truth table of proposed 4 : 2 compressor (Table 2), it can been observed that the error has been introduced for the input values − {0011}, {0100}, {1000} and {1111}, so as to ensure that equal positive and negative deviation with ED = 1 (minimum) is obtained.

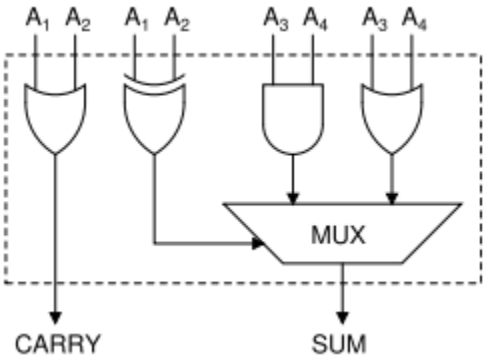

Fig 3. Area-efficient 4:2 compressor.

Brent Kung adder

These are used to take up the binary additions because of their flexibility. Carry Look Ahead Adder's (CLA) structure is utilized in order to get the parallel prefix adders . Tree

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Vol 19, Issue 2, 2025

structures algorithm are used to increase the speed of arithmetic operation. Parallel prefix adders are used for high performance arithmetic circuits in industries as they increase the speed of operation.

The construction of parallel prefix Adder involves three stages:

1. Pre-possessing stage:- Generate and propagate signals to each pair of the inputs A and B are computed in this stage.

Pi = Ai xor Bi

Gi = Ai and Bi

2. Carry generation network:- In this stage, carries equivalent to each bit is calculated. All these operations are implemented and carried out in parallel. Carries in parallel are segmented into smaller pieces after the implementation of the stage. Carry propagate and The operations involved in

CPO = Pi and Pj

CGO = (Pi and Gj) or Gi

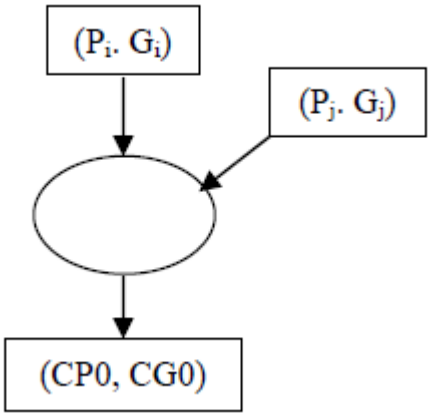

Fig4.Carry network

3. Carry Network Post processing Stage:- This is the concluding step to compute the summation of input bits.

Ci-1= (Pi and Cin)

Si =Pi xor Ci-1

Brent-Kung adder is a very popular and widely used adder . It actually gives an excellent number of stages from input to all outputs but with asymmetric loading of Intermediate stages. It is one of the parallel prefix adders. It is one of the parallel prefix adders where these adders are the ultimate class of adders that are based on the use of generate and propagate signals. In case of Brent kung adders along with the cost, the wiring complexity is also less. But the gate level depth of Brent-Kung adders is 0 (log2 (n)) , so the speed is lower.

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Vol 19, Issue 2, 2025

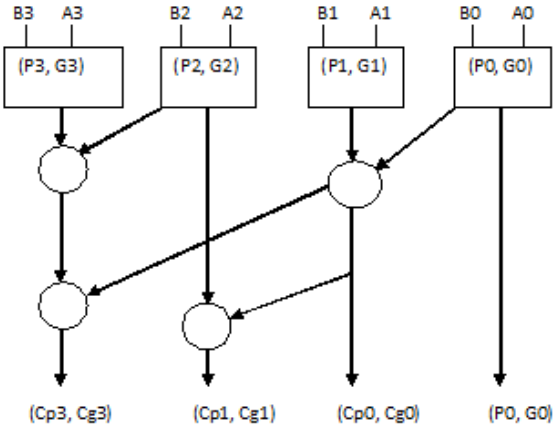

Fig5. 4-bit Brent-Kung adder

IV. RESULTS

RTL SCHEMATIC:- The RTL schematic is abbreviated as the register transfer level it denotes the blue print of the architecture and is used to verify the designed architecture to the ideal architecture that we are in need of development .The hdl language is used to convert the description or summery of the architecture to the working summery by use of the coding language i.e verilog ,vhdl. The RTL schematic even specifies the internal connection blocks for better analyzing .The figure represented below shows the RTL schematic diagram of the designed architecture.

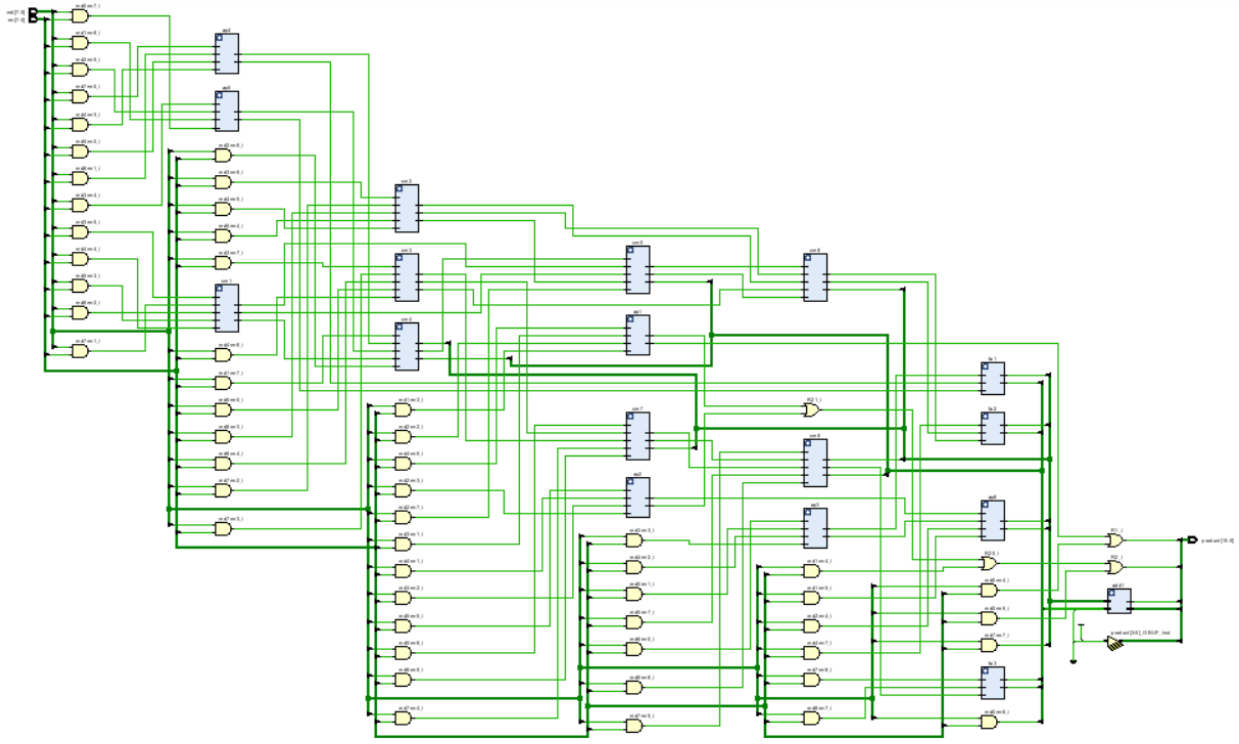

Fig 6 . RTL Schematic of the Proposed Design

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www.ijasem.org
Vol 19, Issue 2, 2025

TECHNOLOGY SCHEMATIC:- The technology schmatic makes the reesentation of the architecture in the LUT format ,where the LUT is consider as the parameter o area that is used in VLSI to estimate the architecture design .the LUT is consider as an squarunit the memory allocation of the code is represented in there LUT s in FPGA

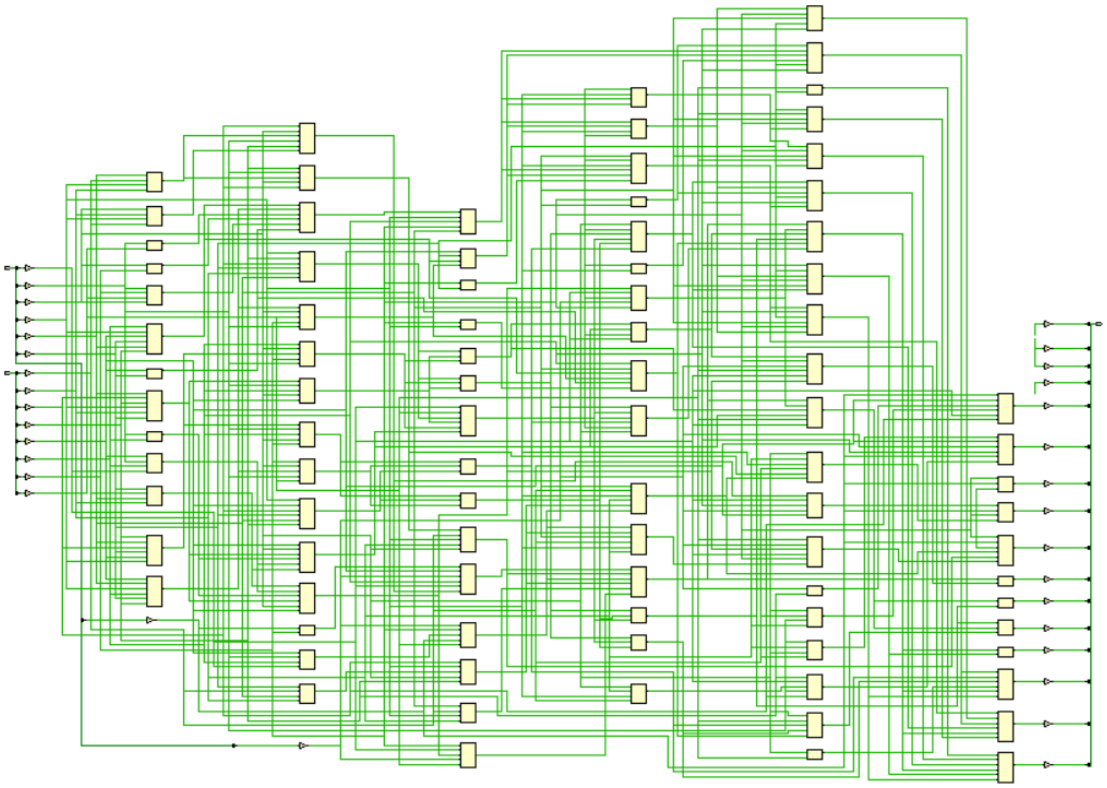

Fig 7. Technology Schematic of the Proposed Design

SIMULATION:-The simulation is the process which is termed as the final verification in respect to its working where as the schematic is the verification of the connections and blocks. The simulation window is launched as shifting from implantation to the simulation on the home screen of the tool ,and the simulation window confines the output in the form of the wave forms. Here it has the flexibility of providing the different radix number systems.

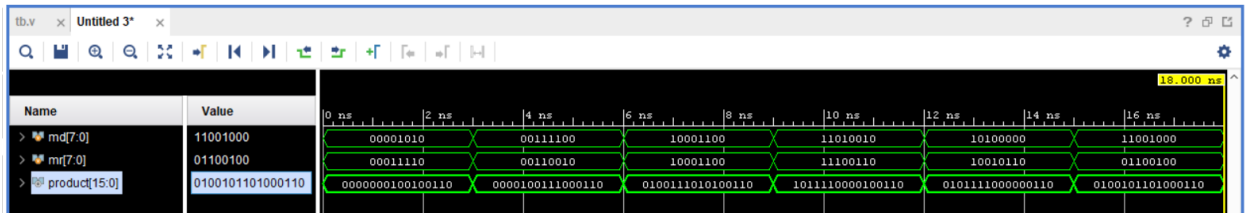

Fig 8. Simaulation wave forms of proposed approximate multiplier

PARAMETERS:-Consider in VLSI the parameters treated are area ,delay and power ,based on these parameters one can judge the one architecture to other.

Parameter	Existing design	Proposed design
No of LUTs	72	67
Power (mw)	10.924	10.189

Table 1 : parameters comparision

V. CONCLUSION

This project presents approximate multiplier with novel approach of approximate 4 : 2 compressor architectures. Firstly, a high speed area and power efficient compressor architecture is proposed, which achieved a considerable reduction in area, delay and power when compared to other state-of-the-art compressor designs. The proposed design has comparable accuracy .As a result, the proposed design reduces area and power. The architecture was designed for image processing applications, like image multiplication and smoothing. In comparison to existing multipliers, the proposed approximate multiplier using brent kung adder offers a significantly more appealing electrical performance.

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