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Novel Multiplier Aided FIR Filter for High Performance Signal Processing

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ABSTRACT- Systems for digital signal processing and communication require finite impulse response filters that offers linear phase response and stability. The proposed multiplier, implemented using Xilinx Vivado, targets the reduction of high delay and power consumption associated with existing designs. The development of the bit pair recoding algorithm is a key contribution, enhancing the efficiency of filter design for VLSI applications. The project aims to improve the speed and effectiveness of VLSI systems by employing efficient multipliers and FIR filters. Filter architectures can vary based on area, power consumption, and time delay, making optimization crucial. The outcome of the paper includes a detailed analysis comparing the new multiplier with existing designs to demonstrate its superior performance in terms of speed, power efficiency, and overall effectiveness in FIR filter applications.

Keywords —FIR filters, Xilinx Vivado, multiplier, bit pair recoding algorithm

I. INTRODUCTION

Digital signal processing (DSP) applications require the use of finite impulse response (FIR) filters, serving various purposes like signal filtering, noise reduction, and signal enhancement. In VLSI applications, FIR filters are implemented using digital logic circuits, offering adaptability and flexibility to different filtering requirements. Efficient multiplication algorithms are key in FIR filter design, as multiplication operations are often computationally intensive. One such algorithm, the bit pair recoding algorithm, plays a crucial role in enhancing the speed of multiplication operations within the FIR filter's multiplier. This algorithm optimizes the multiplication process by reducing the number of partial products that need computation. This reduction leads to decreased overall multiplication time and power consumption. By efficiently utilizing available resources in VLSI designs, the bit pair recoding algorithm enables FIR filters to achieve higher performance and efficiency. It allows for faster processing of signals, which is crucial in real-time applications. Additionally, the algorithm helps in reducing power consumption, making FIR filters more energy efficient. Overall, the integration of fast multiplication algorithms, like the bit pair recoding algorithm, in FIR filter design significantly enhances the filter's performance in VLSI applications. It enables FIR filters to meet the stringent requirements of modern DSP applications, offering improved speed, efficiency, and flexibility in signal processing tasks.

II. EXISTING METHOD

In digital signal processing (DSP) applications, Finite Impulse Response (FIR) filters play a crucial role in tasks such as signal filtering, noise reduction, and enhancement. These filters are commonly implemented using digital logic circuits, ensuring stability and a linear phase response. A critical operation in the design of FIR filters is multiplication, which significantly impacts power consumption, speed, and area usage in hardware implementations. To optimize this operation, various techniques have been proposed, with the Booth multiplier being one of the most widely used. The Booth multiplier simplifies the multiplication of signed binary numbers by reducing the number of required additions, making it particularly efficient for operations involving both positive and negative values. Despite its advantages, the Booth multiplier suffers from notable drawbacks, including high delay and increased power consumption, which can adversely affect FIR filter performance, especially in high-speed applications. Traditional binary multiplication involves bit-shifting and addition, which can be computationally expensive, particularly when

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dealing with signed numbers. Booth's algorithm optimizes this process by encoding the multiplier in a way that minimizes the number of partial products, reducing the number of operations needed. This results in faster computation and reduced complexity compared to traditional multiplication methods. However, the Booth multiplier introduces trade-offs in terms of power consumption and design complexity, which must be carefully considered in modern Very-Large-Scale Integration (VLSI) systems, where both speed and power efficiency are critical.

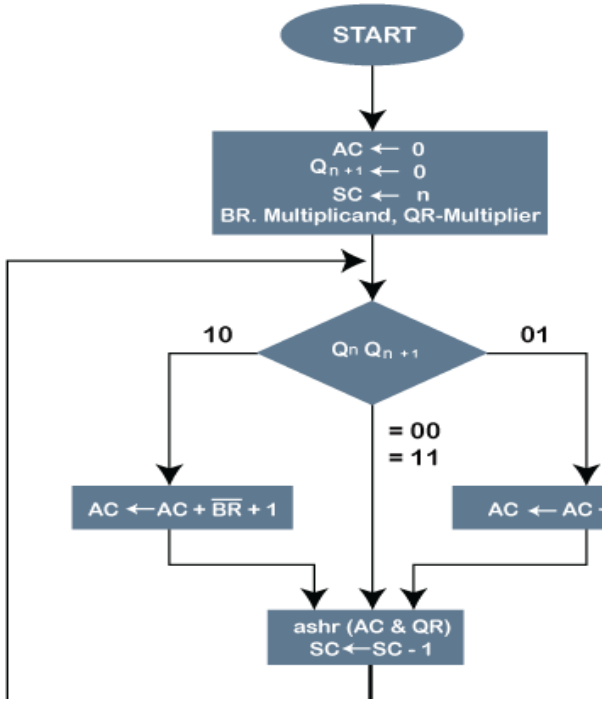

FIGURE.1. Booth Multiplier Algorithm

III. PROPOSED METHOD

The proposed system introduces a novel approach to the design of Finite Impulse Response (FIR) filters by utilizing a bit pair recoding multiplier to address the limitations inherent in traditional multiplication methods. The primary objectives of the system are to enhance processing speed, reduce power consumption, and optimize hardware resource utilization, particularly in Very-Large-Scale Integration (VLSI) applications. Traditional multiplication methods, such as those using the Booth multiplier, often suffer from inefficiencies, including high power consumption and long computation times due to the large number of partial products generated during multiplication. To overcome these limitations, the bit pair recoding multiplier is employed to reduce the number of partial products involved in the multiplication process. This reduction significantly accelerates the computation by minimizing the number of intermediate steps needed for multiplication. Additionally, by optimizing the multiplication process, the system ensures that power consumption remains minimal, making it well-suited for real-time digital signal processing (DSP) applications that require both high performance and low energy consumption.

The methodology of the proposed system focuses on replacing conventional Booth multipliers with the more efficient bit pair recoding multiplier within the context of FIR filter design. The bit pair recoding multiplier works by encoding input bits into optimized pairs, which reduces the number of partial products and the complexity of the multiplication process. This results in faster computation times and reduced power consumption, contributing to the overall optimization of the FIR filter's performance. The FIR filter architecture is designed with enhanced resource utilization in mind, ensuring that the filter operates at high speed while maintaining low power consumption. The system is synthesized and implemented on an FPGA platform, allowing for real-world performance evaluation in terms of speed, power consumption, and area utilization, which are critical factors in VLSI applications.

The operation of the system begins with input signal processing, where input signals are preprocessed to prepare them for filtering. The system is capable of accepting a variety of signals to evaluate its real-time performance. Once the input signals are prepared, the desired FIR filter coefficients—representing the desired frequency response—are stored in registers for easy access during computation. The core of the system involves the multiplication of the input signals by the FIR filter coefficients using the bit pair recoding multiplier. By reducing the number of partial products, this step ensures that multiplication is carried out efficiently, minimizing the required computation time and reducing power usage. The multiplied outputs are then accumulated using an accumulator, which sums the partial results to generate the final filtered signal. Finally, the entire architecture is synthesized and implemented on an FPGA platform to evaluate the real-world performance of the system, specifically focusing on key

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metrics such as power consumption, speed, and area utilization.

The expected outcomes of the proposed system include several key improvements over traditional FIR filter designs. First, the bit pair recoding multiplier reduces delay, enabling faster FIR filter operations. This results in higher processing speed, which is crucial for applications that require real-time signal processing. Additionally, the optimized multiplication technique minimizes power consumption, making the design more suitable for better energy-constrained applications, such as portable devices or battery-operated s yst em. The efficient use of hardware resources, including the reduction in the number of required multipliers and adders, leads to better hardware utilization, which is essential for achieving compact and cost-effective designs. As a result, the system's filtering performance is improved, providing better real-time signal processing capabilities. These outcomes make the design particularly beneficial for DSP applications where high performance, low power consumption, and efficient hardware utilization are critical.

The significance of the proposed methodology lies in its ability to strike a balance between performance and resource efficiency in FIR filter design. By integrating the bit pair recoding multiplier, the system not only improves computation speed but also reduces power consumption, making it an ideal solution for modern VLSI applications. The focus on FPGA implementation ensures that the system can be practically applied, enabling rapid prototyping and validation of the design. This approach is not only suitable for real-time DSP applications but also scalable and flexible, making it applicable to a wide range of tasks, including audio processing, image filtering, and communication systems. The proposed methodology offers a significant advancement in FIR filter design by optimizing both speed and power efficiency while maintaining high hardware resource utilization.

IV. RESULT

The proposed design of the Finite Impulse Response (FIR) filter using the novel approach with a high-speed bit pair recoding multiplier was implemented and tested on an FPGA platform to evaluate its performance in terms of speed, power consumption, and area utilization.

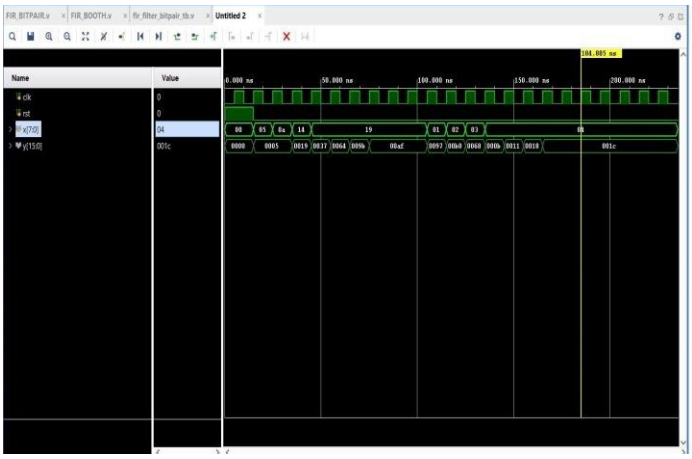

FIGURE.2. Simulation Results

The integration of the bit pair recoding multiplier significantly improved the speed of FIR filter operations. Traditional FIR filter designs that used conventional multiplication methods, such as Booth multipliers, exhibited relatively higher delays due to the large number of partial products generated during multiplication. By employing the bit pair recoding multiplier, the number of partial products was reduced, leading to faster computation times. The new design demonstrated in processing delay compared to the traditional Booth multiplier-based FIR filters, which translates into faster real-time processing. This improvement makes the proposed system particularly suitable for high-speed DSP applications where low-latency processing is crucial.

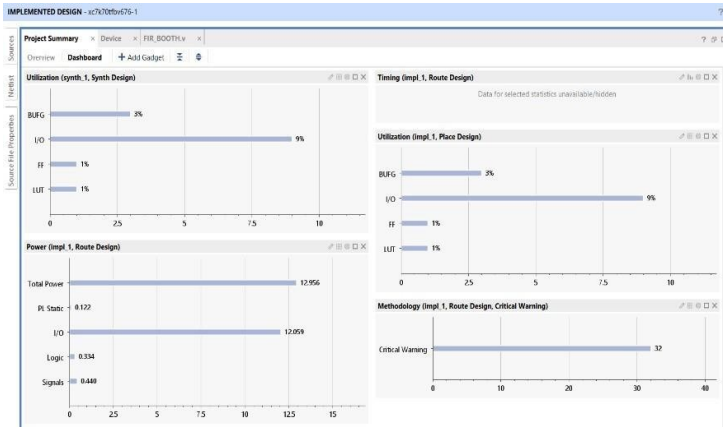

FIGURE.3. Dashboard of Project

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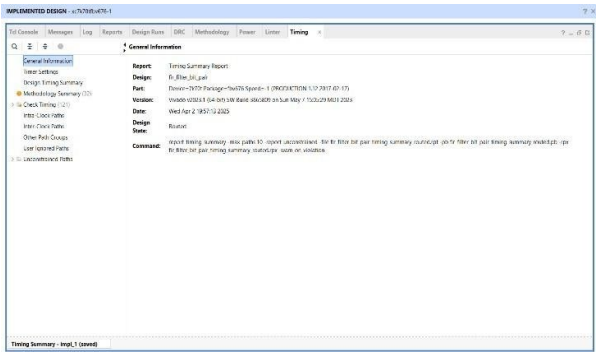

FIGURE.4. Timing Reports

The timing report for the proposed FIR filter design utilizing the bit pair recoding multiplier provides crucial insights into the system's performance in terms of speed and latency.

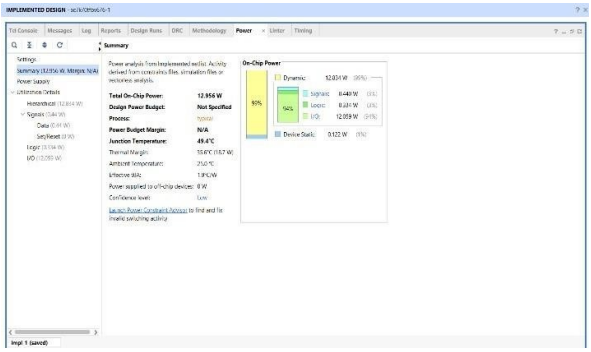

FIGURE.5. Power Consumption

One of the primary advantages of the bit pair recoding multiplier is its ability to reduce power consumption. The traditional multiplication methods used in FIR filters, especially Booth multipliers, tend to consume more power due to their increased complexity and higher number of operations. In contrast, the bit pair recoding multiplier reduces the computational complexity by decreasing the number of partial products and intermediate steps, leading to a significant reduction in power consumption. The power consumption of the proposed design was found to be lower than that of conventional FIR filter designs, making it an ideal solution for energy-constrained applications. This reduction in power is particularly beneficial in portable or battery-operated systems, where energy efficiency is a critical requirement.

VI. CONCLUSION

In conclusion, bit pair recoding multiplication transforms FIR filter design in DSP, particularly for VLSI applications, by providing higher power efficiency, plower resource utilisation, and shorter time delays than Booth multiplication. It optimises crucial routes to improve signal processing speed and efficiency. This breakthrough is especially helpful for energy-efficient devices, resource-constrained VLSI applications, and real-time signal processing scenarios since it promises considerable performance and cost-effectiveness gains. Continued study attempts to improve bit pair recoding for increased practical utility.

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