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Vending Machine for Water with Multipayment using Verilog

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Abstract— With the growing demand for clean and safe drinking water, there is a need for innovative approaches to enhance water access and distribution, particularly in public places like railway stations, where large numbers of people gather and transit daily. This paper presents an FPGA-based vending machine for water, designed to efficiently handle the process of dispensing water and returning change in real-time. The system allows users to select the desired number of liters, the type of water (cold, hot, or normal), and make payments using multiple methods. Unlike traditional vending machines that accept only a single type of input money, this system is enhanced to support multi-denomination payments, including coins and notes. Additionally, it incorporates a card payment system simulated using Verilog-based authentication logic and a QR code-based payment mechanism integrated with an external processor. The outputs of the system include the dispensed water and the correct change returned to the user in real time. By leveraging FPGA technology, this vending machine ensures high-speed transaction processing, flexibility, and reliability, making it a viable solution for smart public utilities.

Keywords— FPGA, Vending Machine, Real-time

I. INTRODUCTION

In an era where convenience, automation, and digital payments are becoming integral to everyday life, the demand for intelligent public utility systems is rapidly increasing. Vending machines, once limited to dispensing snacks and beverages with coin-based inputs, are now evolving into versatile platforms capable of delivering a wide range of services—including access to clean drinking water. However, many existing vending machines still operate on basic hardware models, accepting only singledenomination cash inputs and lacking support for modern payment options.

To address this limitation, this paper presents an enhanced design of a vending machine for water that supports a multipayment system. This upgraded system can accept various denominations of coins and notes, supports card-based payments through simulated authentication logic, and introduces QR code-based payment, integrating with an external processor to verify transactions. These features provide greater accessibility and user flexibility, accommodating the diverse payment preferences of users in public spaces such as stations, schools, and hospitals.

The system is implemented using Verilog HDL and is designed around a Finite State Machine (FSM) architecture that manages user inputs, transaction processing, water dispensing, and change calculation. With real-time response capabilities and modular logic, the design not only ensures a smooth user experience but also demonstrates the potential for future scalability—such as integrating contactless payments, data analytics, and IoT-based monitoring.

By combining the traditional functionality of vending machines with modern digital payment mechanisms, this project aims to bridge the gap between hardware-level control and user-friendly, secure financial interaction. The result is a smarter, more inclusive vending solution tailored for evolving urban infrastructure.

II. LITERATURE REVIEW

Khu et al. [1] pioneered the concept of an FPGAbased intelligent vending machine designed to automate both transaction processing and inventory tracking. Their work emphasized the integration of internal memory modules to monitor product quantities, making the vending system capable of self-updating its stock status. However, the design was limited to basic cash input and lacked adaptability to digital payment systems.

Woon et al. [2] proposed a novel FPGA-driven smart vending machine embedded with health monitoring functionality. Their contribution was notable for combining biomedical sensors with a vending interface, offering realtime diagnostic information. This work demonstrated the potential of FPGA platforms in applications beyond basic dispensing, though the payment logic remained rudimentary.

Kuan et al. [3] addressed the challenges specific to **water** vending machines, especially the control of liquid flow, measurement accuracy, and error handling. Their FSM design allowed precise control of valves and volume-based dispensing, making their model highly relevant for waterbased utility systems.

El Sayed and Asyali [4] introduced a vending machine system that could dispense multiple types of products. Their reconfigurable design used Verilog to handle various inputs and outputs associated with different goods. Although the design showed strong adaptability, it still used traditional coin-based inputs.

Ansari and Sheikh [8] built a vending controller for deployment in public environments, emphasizing reliability, user safety, and secure interface design. Their approach considered physical security and user ergonomics but did not incorporate advanced transaction methods such as card or mobile payments.

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Mahmood and Ahmad [9] developed a reconfigurable vending machine, showing how FPGA's flexibility could allow vendors to modify machine behavior without changing the hardware. Their work paved the way for future extensibility but remained focused on reprogramming for product variety, not payment options.

Kho and Kumar [10] proposed a system for dispensing integrated circuits (ICs) via vending logic. Their design required fine-tuned control to handle delicate components, showing FPGA's application in specialized environments.

However, payment flexibility was not a focal point.Suthar [11] and Sathiyapriya et al. [12] contributed modular FSM architectures and Mealy model-based vending logic, simplifying complex state transitions and improving the readability and maintainability of FSM designs.

Verma [13] performed a comparative study between FSM modeling styles, providing valuable insights into logic optimization, design complexity, and timing behavior. This helps designers choose between Moore and Mealy implementations for specific application constraints.

Guo and Liu [14] introduced hybrid architectures combining FPGA with microcontrollers. Their vending machine achieved better software control through microcontroller integration while retaining real-time processing in FPGA. Yet, their payment logic did not extend beyond traditional coin validation.

Megalingam et al. [5][6][7] extended FSM-based Verilog applications into areas such as medical monitoring, assistive technologies, and autonomous mobility, validating FSM's power in managing complex control flows, which aligns well with the needs of a multi-path payment transaction system.

Verma et al. [15] investigated low-power FSM implementations, introducing energy-saving techniques such as clock gating and state suppression, crucial for batterypowered or solar-operated vending installations.

Despite the range of advancements, few studies have attempted to create a multi-payment vending machine using Verilog HDL. Most existing works either focused on physical product diversity, user interface improvements, or control precision. However, the integration of multiple transaction methods—including cash (coins/notes), card verification logic, and QR code scanning— remains largely unexplored in Verilog-based vending machines.

The current work bridges this gap by proposing a comprehensive, FSM-driven design that not only supports multiple payment types but also simulates authentication and integrates external signals (QR scan success). The design provides a scalable base for future extensions, including contactless payment modules, transaction logging, and multiproduct vending through modular Verilog blocks.

III. SYSTEM ARCHITECTURE

The architecture of the proposed vending machine system is designed using a modular Finite State Machine (FSM) approach, which provides deterministic control flow and predictable state transitions. This FSM is implemented using Verilog HDL and mapped onto FPGA hardware. The key objective of this architecture is to simulate real-world vending scenarios while accommodating multiple payment methods in a structured, hardware-centric environment.

The system consists of five major functional blocks:

I. **Input Handler**:
Captures user inputs including the number of litres to be dispensed, the water type (normal, cold, or hot), and the selected payment method. Debouncing logic is applied to ensure stability in button and switch inputs.

II. **FSM Controller**:
Acts as the brain of the system. It processes user selections and transitions through various logical states such as IDLE, SELECTION, VALIDATION, DISPENSING, and RETURN. This controller ensures that the vending process flows logically and handles invalid or incomplete inputs by reverting to the IDLE state.

III. **Payment Processing Unit**:
This block determines whether a transaction can proceed based on the payment mode: • For **cash**, it compares the entered amount with the required amount.

- For **card**, a simulated balance register is used to verify whether sufficient funds exist.
- For **QR payments**, an external pulse or signal is interpreted as a successful scan and validation.

IV. **Change Calculation and Control Logic**:
If the entered payment exceeds the required amount, this block calculates and activates the return of change. In the case of card payments, it deducts the amount from the simulated balance.

V. **Dispense and Output Controller**:
Once the payment is validated, this unit activates the dispense signal and optionally displays messages or status using LEDs or output pins.

Together, these modules form a robust, reusable, and scalable hardware system that mimics real-world vending logic.

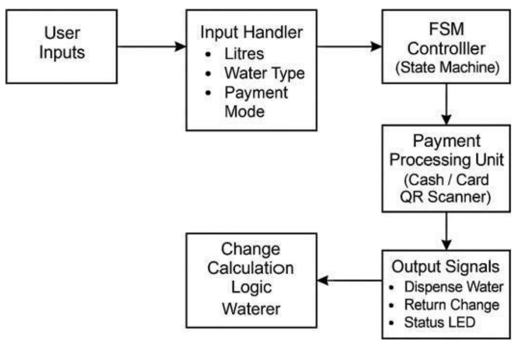

Fig. 1. Block diagram of water vending machine system

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IV. DESIGN AND IMPLEMENTATION

The system is implemented using behavioral modeling in Verilog, where state logic is encoded using enumerated types and case constructs. Clockdriven state transitions and input evaluation ensure synchronous operation and timing accuracy. FSM Design Principles: • The IDLE state initializes the machine and waits for user interaction.

- In SELECT_LITRES, the input value is verified against allowed values (1, 2, 5, 10 litres).
- The SELECT_WATER_TYPE state ensures a valid type selection: normal, cold, or hot.
- SELECT_PAYMENT_MODE allows users to choose between cash, card, or QR code.
- In VALIDATE_PAYMENT, internal logic checks input sufficiency based on the selected mode.
- DISPENSE_WATER is triggered if validation passes.
- RETURN_CHANGE handles change computation and resets the machine for the next transaction. • Each transition is triggered on a positive clock edge and depends on valid input conditions.

Verilog Modules: • vending_machine.v: Top-level FSM integrating all submodules.

- payment_logic.v: Encapsulates cash and card validation logic.
- qr_interface.v: Interprets input from external processor for QR scan.
- change_calc.v: Computes change using simple arithmetic subtraction logic.
- dispense_control.v: Controls the water dispense signal and visual indicators.

Testbenches were written for individual modules and the top-level FSM to ensure modular functionality.

V. SIMULATION AND RESULTS

A. Behavioral Simulation

Simulation of the vending machine FSM was performed using the Vivado simulation tool. A comprehensive testbench was developed to simulate various transaction types, input combinations, and invalid scenarios. The waveform shows state transitions, signal activations, and output correctness across all cases.

Key results:

- The dispense signal was correctly asserted when the payment matched or exceeded the required amount. • The change output accurately reflected the excess amount entered.
- For card and QR payments, the FSM waited for valid authorization signals before proceeding.
- Test cases covered:
- Cash payments with exact and excess amounts
- Card payments with valid and insufficient balances
- QR code transactions simulated by external signals
- Invalid litre or water type selection

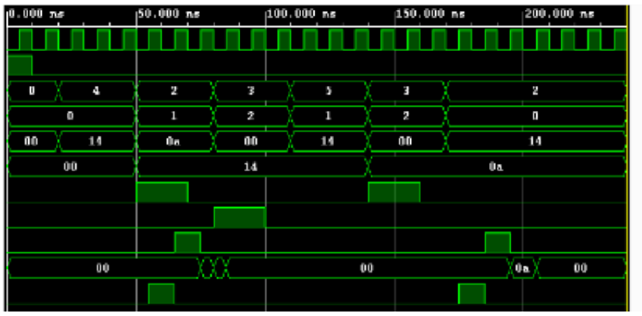
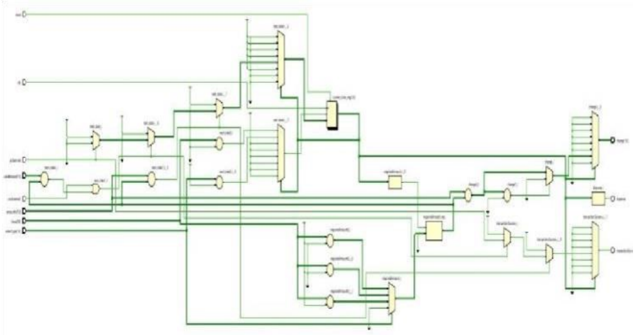


Fig. 2: Simulation Waveform showing state transitions and outputs

B. RTL and Technology Schematic

The **RTL schematic** verifies correct instantiation of logic modules. FSM logic is clearly segmented into flip-flopbased sequential blocks and MUX-based decision structures.

The **Technology schematic** illustrates how the



design maps into FPGA primitives, such as Look-Up Tables (LUTs), Flip-Flops (FFs), input buffers, and output drivers. Each FSM state is implemented as a memory-like element, confirming hardware realization.

Fig. 3: RTL Schematic of vending machine

C. Synthesis and Resource Utilization

Postsynthesis resource utilization showed efficient FPGA resource usage:

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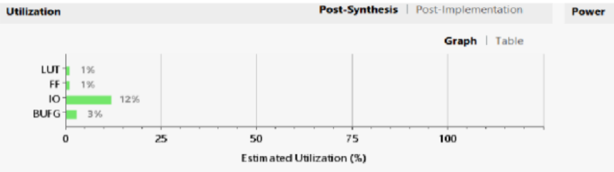

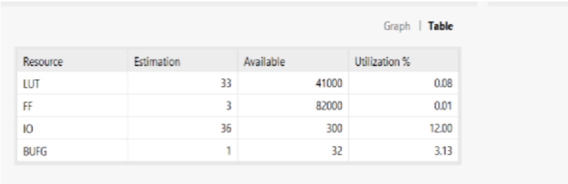

Resource	Estimation	Available	Utilization %
LUT	33	41000	0.08
FF	3	82000	0.01
IO	36	300	12.00
BUFG	1	32	3.13

Fig. 4: Resource Utilization after Synthesis

VI. FUTURE WORK

The current system offers a strong foundation for further enhancements. Some proposed future extensions include:

1. Mobile Wallet and UPI Integration: The payment module can be extended to support digital wallets and contactless payments using lowcost communication interfaces. This will make the machine more compatible with cashless environments.
2. Central Transaction Logging: A simple memory buffer or register file can be added to store recent transactions, which could be periodically read by maintenance personnel or interfaced with an external processor.
3. Multi-Product Vending Extension: By adding a product selector and extending the FSM with additional pricing logic, the system could support multiple water products or beverages, enhancing usability in commercial environments.

These improvements can be added without redesigning the core FSM, proving the modularity and flexibility of the current implementation.

VII. CONCLUSION

This paper presents the development and implementation of a smart, multi-payment water vending machine using Verilog HDL. The FSMbased system supports multiple denominations of coins and notes, card-based transactions using simulated logic, and QR code payments via external triggering. The system was synthesized, simulated, and analyzed for functionality, timing, and hardware efficiency.

Simulation results confirm the accuracy of the transaction flow, output handling, and FSM transitions. Post-synthesis analysis reveals that the design uses minimal hardware resources, making it ideal for deployment on compact and cost-effective FPGA platforms.

With scalable architecture and modular FSM control, this design can evolve to handle complex vending tasks and advanced user interactions in future iterations.

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