ISSN: 2454-9940

INTERNATIONAL JOURNAL OF APPLIED SCIENCE ENGINEERING AND MANAGEMENT

E-Mail :
editor.ijasem@gmail.com
editor@ijasem.org

www.ijasem.org

INTERNATIONAL JOURNAL OF APPLIED SCIENCE ENGINEERING AND MANAGEMENT

ISSN 2454-9940

www.ijasem.org

Vol 19, Issue 2, 2025

ADVANCED MULTILEVEL INVERTER TOPOLOGY FOR RENEWABLE ENERGY TRANSFORMATION

B.Durga naik Asso. Pro.
Department of EEE

M.China lal Asso. Pro.
Department of EEE

A.Venkatesh Assi. Pro.
Department of EEE

T.Srinivasarao
P.Agasthya
N.Nithin
T.Saipraneeth
Department of EEE
TKR College of engineering and technology
Meerpet, Saroornagar, Hyderabad

***Abstract*—This paper presents a new three-phase integrated module multilevel inverter (IMMLI) with reduced component count which is suitable for low, medium and high voltage renewable energy systems. The proposed inverter is a resultant structure of a number of integrated module and each module is configured with a number of series connected basic blocks. Each block consists of a dc voltage source, a blocking diode and a semiconductor switch. A computational combination and summation among the dc sources from different blocks results in a high number of levels within the output voltage. This task is performed by controlling the switches equipping appropriate switching algorithm. Thus, a high level of output is obtained employing reduced number of components. Since the topology owns two degree of modularity, the total stress voltage (TSV) of the system is low and distributed among the switches. Hence, the proposed topology allows to be implemented in high power systems with reduced amount of costs. The inverter also offers enhanced efficiency, as the number of simultaneously conducting switch is low. Additionally, in order to operate the presented inverter with optimum ac power quality, a multi-carrier based level shifted PWM scheme is addressed in this paper. This paper also shows how to prepare balanced dc sources that are required to implement the inverter using high-frequency magnetic-link. The operating principle of the IMMLI is explained with the help of a fifteen level (15-L) single phase unit and its performance is evaluated in MATLAB/Simulink considering different conditions. Simulation results and to evaluate its superiority over the existing.**

***Index Terms*—total harmonic distortion (THD), integrated module multilevel inverter (IMMLI), maximum stress voltage (MVS), total stress voltage (TSV).**

I. INTRODUCTION

Electric and electronic loads are being multiplied rapidly with the increase in total number of population. Accordingly, a huge amount of electrical energy is required to be generated to face the ongoing energy-demand [1], [2]. Source of unlimited energy, *i.e.*, renewable energy sources like solar, wind, ocean, and hydrogen fuel cell are actively participating in this energy generation endeavor, and the process includes several intermediate energy conversion stages such dc-dc, dc-ac, ac-dc, and ac-ac transformation [3], [4], [5]. All of the stages are necessary based on specific application areas. However, the dc-ac conversion stage is more crucial than others, since electrical energy is generally transmitted in the form of ac power. Thereby, the device that performs the role of dc-ac conversion, known as inverter is a vital element in the field of electrical power [6].

Different types of inverter have been introduced by the researchers so far including two level square-wave inverter, transformer less inverter, quasi z-source inverter, and multilevel inverter (MLI) [7], [8]. However, in case of renewable energy harvesting, MLIs are considered as the irreplaceable individual, as it distributes the total voltage and current stresses across the semiconductor devices into small part. Thus, it obtains more reliability as well as durability while applied in high voltage renewable energy systems (RESs). Moreover, MLI produces PWM stairs in the output resulting in better quality ac power without equipping any filter components [9]. Thus, it becomes light-weighted and small size, and reduces the cost of filter components. However, most of the recently developed MLI topologies meeting the aforementioned challenges suffer from high TSV. This is because, a reduced number of switches are employed to develop the design, which have high voltage stresses. For the same reason, the total cost of the inverter also increases, as high rated switches cause high cost. Furthermore, the higher the number of switch operating with maximum voltage stress (MVS), the higher the switching losses, and the lower the application compatibility of the inverter for high power systems [10]. Therefore, creating a perfect trade-off between the design, and the corresponding cost, TSV, power quality

ISSN 2454-9940
www.ijasem.org
Vol 19, Issue 2, 2025

and efficiency of an MLI may be considered as an essential objective.

Multilevel inverters have gained widespread attention for their ability to improve power quality, reduce harmonic distortion, and enhance energy conversion efficiency in renewable energy applications. Over the years, several inverter topologies have been proposed, each offering distinct benefits and challenges.[1] explored the performance of diode-clamped multilevel inverters in photovoltaic systems, highlighting their efficiency in reducing switching losses and maintaining power stability. However, the increased complexity of diode clamping circuits poses a design challenge. Similarly, cascaded H-bridge inverters, studied by [2], provide a more modular and scalable solution for high-power applications, but the cost and complexity increase with the number of levels used.[3] analyzed the role of flying capacitor multilevel inverters in renewable energy systems, emphasizing their capacity to handle higher voltage levels with minimal harmonic distortion. However, managing the large number of capacitors remains a critical issue. [4] Investigated the use of hybrid multilevel inverters that combine different inverter topologies to improve both performance and cost-efficiency, making them suitable for grid-connected renewable energy systems.

Recent research has focused on improving the control strategies of multilevel inverters to optimize energy efficiency and power quality. [5] Proposed an advanced pulse-width modulation (PWM) technique that reduces total harmonic distortion (THD) while maintaining low switching losses. [6] Developed an optimized switching strategy for multilevel inverters used in wind energy systems, improving energy conversion efficiency under fluctuating wind conditions. [7] explored the integration of model predictive control (MPC) with multilevel inverters, demonstrating significant improvements in dynamic response and load handling. Despite advancements in multilevel inverter technology, challenges remain. [8] pointed out the limitations in scalability for high-level inverter designs due to increased component count and complexity. [9] explored the reliability issues associated with multilevel inverters, particularly the increased likelihood of component failure in high-power applications. [10] discussed the importance of optimizing inverter topologies to reduce the size and cost of passive components, which remain a barrier to widespread adoption. More recent efforts, such as those by [11], have looked at integrating machine learning techniques to improve the fault tolerance and predictive maintenance of multilevel inverters in renewable energy systems. [12] suggested that the use of adaptive control strategies could further enhance the reliability and efficiency of these systems, paving the way for their wider deployment in grid-connected solar and wind power applications.

The concept of multilevel inverters was introduced to address the limitations of traditional two-level inverters, which generate only two voltage levels (high and low). Multilevel inverters, on the other hand, generate a stepped output voltage by combining multiple voltage levels. This approach not only reduces switching losses but also minimizes harmonic distortion in the output waveform. Multilevel inverters can be classified into several topologies, including the diode-clamped, flying capacitor, and cascaded H-bridge inverters, each offering distinct advantages in terms of performance and application suitability. In renewable energy systems, the use of multilevel inverters has proven to be highly effective in improving power quality. For instance, in photovoltaic (PV) systems, where the variability of solar irradiance can cause fluctuations in output power, multilevel inverters help stabilize the voltage and reduce harmonic distortion. Similarly, in wind energy systems, where wind speeds fluctuate, multilevel inverters ensure smoother power delivery and enhance the efficiency of the energy conversion process. Despite their advantages, multilevel inverters pose certain challenges, including complex control strategies and increased component count, which can lead to higher costs and reliability concerns. To overcome these issues, research has focused on optimizing the design and control strategies of multilevel inverters, including advanced pulse-width modulation (PWM) techniques and optimal switching sequences. By addressing these challenges, multilevel inverters can continue to play a critical role in the integration of renewable energy sources into the grid, ensuring high power quality and efficient energy conversion. The remainder of this paper is organized as follows: Section II provides a detailed overview of multilevel inverter topologies and their applications in renewable energy systems. Section III discusses the design and optimization techniques for improving inverter performance, focusing on harmonic reduction and power quality. Section IV presents the simulation setup and results, highlighting the efficiency and effectiveness of the proposed multilevel inverter design. Finally, Section V concludes the paper with a summary of key findings and suggestions for future research directions in the optimization of multilevel inverters for renewable energy applications.

INTERNATIONAL JOURNAL OF APPLIED SCIENCE ENGINEERING AND MANAGEMENT
ISSN 2454-9940
www.ijasem.org
Vol 19, Issue 2, 2025

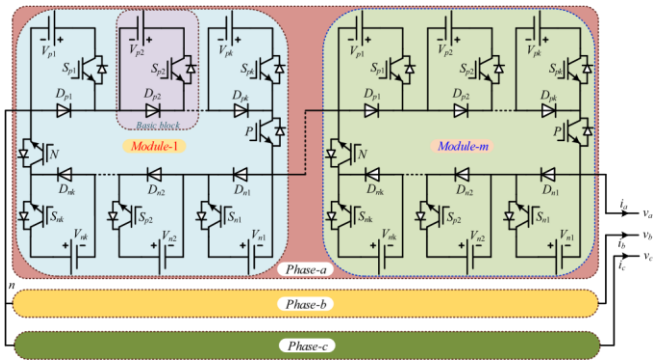

Fig. 1. Generalized circuit diagram of the proposed three-phase integrated module multilevel inverter.

II. Proposed Multilevel Inverter

A. Generalized Circuit Configuration

Massive worldwide energy demand has led to significant usage of fossil fuels, which has affected the environment by increasing greenhouse gas emissions. So, renewable energy resources have gained popularity and growth through producing clean electricity.

PV cells are used in solar-based technologies to transform the sun's energy into usable power. Figure 2 describes the operation of photovoltaic cells, converters, inverters, and energy control units that make up a system for converting solar energy. Nevertheless, efforts are being made to better understand how to incorporate renewable energy sources into the electricity grid. There has been an increased focus on power converters and their controls because of the importance of their work in transforming electricity and controlling the output power. DC–DC converters are typically used in the initial stage of integrating renewable energy sources into a DC grid. Due to the output voltage variations of renewable energy sources such as wind and solar PVs, this stage must operate at peak efficiency. Hence, it is imperative that the DC–DC converters in the front-end stages exhibit responsive behavior towards such fluctuations in order to operate at their optimal efficiency. In small-scale industrial or utility applications, these inverters are frequently employed because of their elevated voltage stress, poor efficiency, elevated operating temperature, and increased pressure capabilities. Multiple inverters are commonly utilized in large-scale, high-power, grid-connected renewable energy systems due to their advantageous characteristics.

No. of output voltage levels: $N_L = 2^{k+1}m - 2m + 1$ (1)

No. of switches for each phase: $N_{sw} = 2m\,(k+1)$ (2)

No. of asymmetric DC sources and power diodes required for each phase:

$$N_{dc/dio} = 2km \quad (3)$$

And the sequential values of the asymmetric DC sources in every module can be determined by:

$$V_{pk} = V_{nk} = 2^{k-1}V_{in} \quad (4)$$

Where, k and m are positive integers with $k = m = 1, 2, 3\ldots$ Accordingly, for a 15-L single phase unit, the value of m and k can be assumed as 1 and 3, respectively. Hence, 6 asymmetrical DC sources are needed whose magnitudes are defined as,

$$\begin{aligned} V_{p1} &= V_{n1} = V_{in}\,|_{k=1} \\ V_{p2} &= V_{n2} = 2V_{in}\,|_{k=2} \\ V_{p3} &= V_{n3} = 4V_{in}\,|_{k=3} \end{aligned} \quad (5)$$

Where, V_{in} represents the fundamental value of the applied dc source. Apart from these, the stress voltage of each switch inside a block equals to the voltage of dc source with which it is connected in series. Thus, the maximum stress voltage (MVS) of the inverter equals to $(2^k - 1)V_{in}$. Thus, the TSV of a single-phase leg of the proposed inverter can be expressed as follows:

$$TSV = 4m \sum_{k=1,2,3\ldots} (2^k - 1)V_{in} \quad (6)$$

here, m is identified as the number of integrated module in each phase. If k is limited to 3, a module is obtained with only 8 switches that can provide 14-L output along with $7V_{in}$ (*i.e.*, ~3.5 kV if V_{in} is set to 500 V) of MVS. Since the approximate maximum value of tolerable stress voltage of a switch available in the market is 6.5 kV, the resultant module allows a cascaded structure of the inverter for applying in the medium and high-power renewable energy systems as a result. Therefore, analyzing the above equations, it is clear that the proposed inverter is capable of generating higher level output (*i.e.*, better quality ac power) employing reduced number of components, and stands with minimized equipment costs, as it offers cascaded configuration with the switches that have practically low stress voltage.

However, the entire system configuration with 15-L proposed inverter unit is illustrated in Fig. 2, where a common dc bus is formed with different types of renewable energy sources along with the storage devices. The terminal voltages of each PV panel and wind farm are maintained at the dc bus voltage by controlling the respective dc-dc converter connected to each source as shown in Fig. 2. An external storage device is also connected to the bus in parallel to store the additional energy for backup. In this way, a

INTERNATIONAL JOURNAL OF APPLIED SCIENCE ENGINEERING AND MANAGEMENT
ISSN 2454-9940
www.ijasem.org
Vol 19, Issue 2, 2025

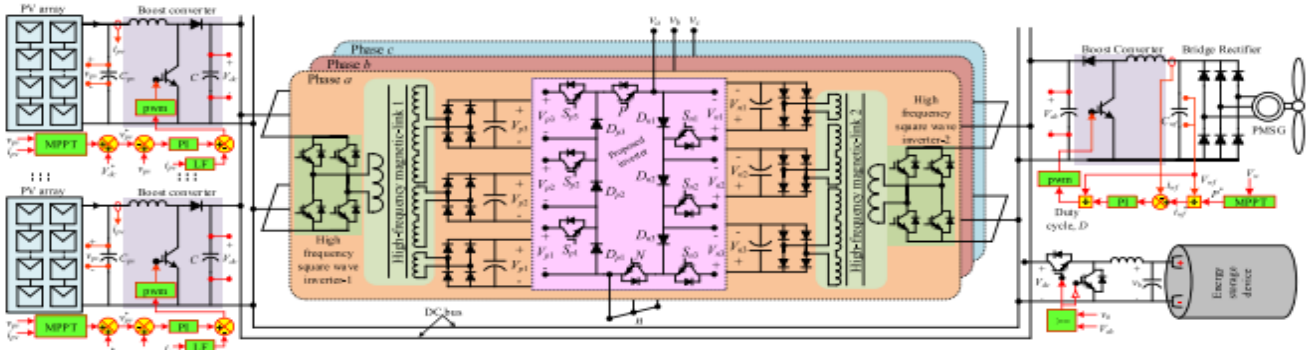

Fig. 2. Schematic diagram of the entire system connecting 15-L proposed inverter unit to two different renewable energy sources along with a storage device

common dc bus with balanced terminal is constructed with the system. However, this figure also illustrates a concept of dc source development using high-frequency magnetic-link. It can be confirmed from Fig. 2 that, for a 15-L single-phase inverter unit, each half converter (*p*- or *n*-converter) requires three asymmetrical dc sources which are obtained from the three asymmetrical secondary windings ($n_1 = n_p / n_{s1} = 1$, $n_2 = n_p / n_{s2} = 0.5$,and$n_3 = n_p / n_{s3} = 0.25$)of a magnetic-link through a rectification process. Since a single magnetic-link is responsible for preparing the dc sources needed in each half converter, six magnetic-links are employed in total to obtain all the dc sources required for the three-phase systems. Moreover, every magnetic link is equally energized with the help of a high-frequency square-wave inverter, whose input power is controlled through an equal power sharing algorithm, as depicted in Fig. 3. Since the input power of the high-frequency square wave inverter is transferred to the three asymmetric dc-links through a transformer action, all the dc-link voltages are tightly regulated at the ir required values employing the algorithm shown in Fig. 3. The left portion of Fig. 2 represents the entire power balance control scheme and the right portion defines how the controller works. This algorithm continuously measures all the dc-link voltages to maintain them at their desired level equipping the voltage regulator loop as shown in the upper-right portion of Fig. 3. However, although the voltages across the dc-links are asymmetrical in values, each source is responsible to deliver equal power, which is confirmed by the power balance loop, shown in the lower-right portion of Fig.2. In the power balance loop, $P_{dc}/3$ (P_{dc}= input power of square wave inverter) is subtracted from the power delivered by each source (P_{in1}, P_{in2} and P_{in3}) to obtain the error signals, which are shortly passed through the low-voltage direct current (LVDC) control blocks.

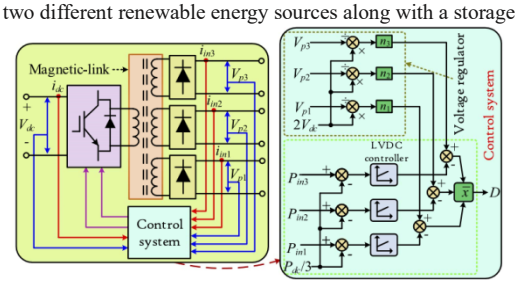

Fig. 3. Complete control scheme along with the switching algorithm for a 15-L single-phase inverter unit.

Then, the resultant signals are subtracted from the signals obtained by the voltage regulator loop providing duty ratios. The final duty ratio (D) to generate PWM signals for that specific square inverter is achieved by averaging all the three duty ratios. Accordingly, this algorithm also confirms equal power sharing among different square wave inverters as well as among the magnetic-links. Therefore, it can be estimated that the system shown in Fig. 2 is capable of harvesting renewable energy from various parallel connected renewable energy sources, and able to deliver balanced ac power to the load.

B. Control Scheme and Switching Algorithm

This section explains a control scheme along with a switching algorithm that has been employed to generate the gate driving signals and to connect the inverter to the grid. The active and reactive power of the proposed inverter is controlled by equipping PI controller, shown in Fig. 3(b). This control diagram contains two parts including outer voltage regulator and inner current loop. Firstly, the active power is controlled by generating reference *d* component of the current (i_d^*) with the help of the voltage control loop in which the reference dc voltage (V_{dc}^*)is compared with the measured V_{dc}. The error signal used to calculate$i_d^*$is transferred through a PI controller with gains K_p= 5.9 and K_i = 790. The measured i_d component obtained from the measured grid current is subtracted fromi_d^* and the resultant signal is applied to a PI controller with gains K_p= 0.45 and K_i = 25. As a result, v_d^* is obtained after a comparison with the measured $v_d$and a component multiplied

INTERNATIONAL JOURNAL OF APPLIED SCIENCE ENGINEERING AND MANAGEMENT
ISSN 2454-9940
www.ijasem.org
Vol 19, Issue 2, 2025

by the gains. Here, R_r and L_r represent the internal resistance and inductance of filter inductor. On the other hand, the reference q component of the voltage is calculated by the inner current control loop. The Q^* in the current loop represents the reactive power demanded by the consumers connected to the grid.

This reactive power is compared to the measured Q supplied by the inverter and a resultant $i^*_q$is achieved through a PI controller with gains K_p=0.45andK_i = 25. The i_d component of the grid current is subtracted shortly from $i^*_q$and passed through a PI controller, which participates to obtain v_q^*. Combination of the two reference dq components of the voltage results a controlling reference signal that is used to control the active and reactive powers of the inverter supplied to the grid. Nevertheless, the reference signal is compared to a zero voltage level to generate 50 Hz pulse with the P switch.

The pulse for N switch is obtained from is verse comparison. To generate pulses for other switches, the obtained reference signal is transformed to make it unipolar and then compared with N_c number of carrier signals. Here, N_c is dependent upon N_L and calculated based on (7). The amplitude of each carrier signal is determined using the equation demonstrated in (8). Based on the upper (7), it can be assumed that 7 carrier signals are needed in total to generate seven intermediate modes by comparing with the unipolar reference signal. Every intermediate mode except the 7th, multiplied by the inverted version of the signal next to it results in desired operating modes, *i.e.*, m_1-m_7. Finally, a fair combination of the operating modes becomes responsible for the resultant gate driving signals (*e.g.*, S_{p1}-S_{n3}), as illustrated in Fig. 3(c). However, the operating modes of a 15-L single-phase proposed inverter are listed in Table I with respective load current path, stress voltage, and output voltage. Based on the Table I, operating principle of the proposed 15-L inverter is explained in details.

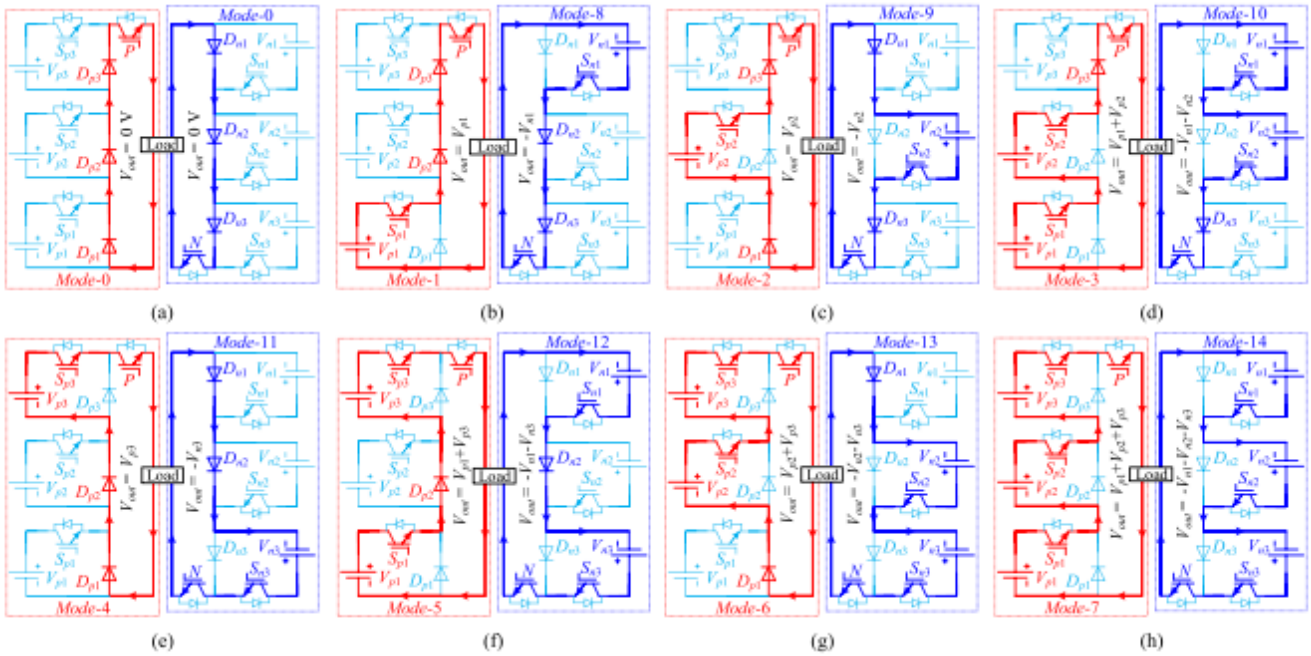

Fig. 4. Operating modes of the proposed 15-L single-phase inverter unit

$$N_c = \frac{N_L - 1}{2} \tag{7}$$

$$A_C = \frac{A_{ref}}{N_c} \tag{8}$$

C. Operating Principle

This section covers up the operating principle of the proposed inverter with appropriate circuital diagram as shown in Fig. 4. As presented earlier in Table I that a 15-L inverter unit is able to generate 15 different operating modes such as *Mode*-0 to *Mode*-14. Half of the modes (*i.e.*, *Mode*-1 to *Mode*-7) occur during positive half-cycle of the output voltage generated by *p*-converter, and the rest halves are obtained during negative half-cycle with *n*-converter. In the following, the pair of similar working modes are explained linearly with an aim to explore all of the modes. *Mode*-0: This mode, shown in Fig. 4(a), is obtained by only turning on either switch P or N. All the other switches remain unpowered during this mode resulting in zero output voltage at the load terminal.

Mode-1 &*Mode*-8: These two modes are similar in nature as shown in Fig. 4(b) except individual's acting slot. S_{p1} &P,

INTERNATIONAL JOURNAL OF APPLIED SCIENCE ENGINEERING AND MANAGEMENT
ISSN 2454-9940
www.ijasem.org
Vol 19, Issue 2, 2025

and S_{n1} &N switches conduct during *Mode*-1 and *Mode*-8, respectively, providing output voltage equivalent to,

$$V_{out} = V_{p1} = V_{in} \quad (9)$$

$$V_{out} = -V_{n1} = -V_{in} \quad (10)$$

Mode-2 &*Mode*-9: During these modes, V_{p2} and V_{n2} are connected to the load through the conduction paths provided by S_{p2}, &P, and S_{n2} &N, respectively. D_{p2} and D_{n2} act as blocking diodes during respective mode. These two modes are demonstrated in Fig. 4(c). The obtained output voltage during respective mode is,

$$V_{out} = V_{p2} = 2V_{in} \quad (11)$$

$$V_{out} = -V_{n2} = -2V_{in} \quad (12)$$

Mode-3 &*Mode*-10: During each of the modes, two voltage sources are connected in series by turning on three switches simultaneously as illustrated in Fig. 4(d). For example, V_{p1} and V_{p2} are added with active S_{p1}, S_{p2} and P during *Mode*-3. On the other hand, S_{n1}, S_{n2} and N are responsible for summing V_{n1} and V_{n2} voltages during *Mode*-10. Therefore, resultant output voltage during individual mode becomes,

$$V_{out} = V_{p1} + V_{p2} = 3V_{in} \quad (13)$$

$$V_{out} = -(V_{n1} + V_{n2}) = -3V_{in} \quad (14)$$

Mode-4 &*Mode*-11: During *Mode*-4 as depicted in Fig. 4(e), V_{p3} is connected to the load with two switches, S_{p3} &P. On the other side, S_{n3} &N remain ON state to attached V_{n3} to the load terminal during *Mode*-11. Consequently,

$$V_{out} = V_{p1} + V_{p2} = 4V_{in} \quad (15)$$

$$V_{out} = -(V_{n1} + V_{n2}) = -4V_{in} \quad (16)$$

Mode-5 &*Mode*-12: In these modes as illustrated in Fig. 4(f), the first and third voltage sources inside each half-converter are cascaded by employing their respective series-connected active switches, and contacted to the load terminal with P or N, respectively. For instance, V_{p1} and V_{p3} are added by turning on S_{p1} and S_{p3}, where active S_{n1} and S_{n3} sum up V_{n1} and V_{n3} voltages. Thus, output voltage during these modes is,

$$V_{out} = V_{p1} + V_{p3} = 5V_{in} \quad (17)$$

$$V_{out} = -(V_{n1} + V_{n3}) = -5V_{in} \quad (18)$$

Mode-6 &*Mode*-13: During *Mode*-6, S_{p2}, S_{p3} and P switches are turned-on to add the voltages of V_{p2} and V_{p3}, and to transfer the obtained voltage to the load. On the other hand, V_{n2} and V_{n3} are summed and connected to the load with the help of S_{n2}, S_{n3} and N switches during *Mode*-13. Both of the modes can be seen in Fig. 4(g). As a result, the output voltage during each mode is determined as,

$$V_{out} = V_{p2} + V_{p3} = 6V_{in} \quad (19)$$

$$V_{out} = -(V_{n2} + V_{n3}) = -6V_{in} \quad (20)$$

Mode-7 &*Mode*-14:

In *Mode*-7, all the switches of *p*converter are turned on to achieve summarized voltage from all three respective sources. Similarly, a cascaded voltage is obtained from all three sources of *n*-converter in *Mode*-14 when all the switches remain ON state. Both of the modes can be confirmed from Fig. 4(h). Thereby, the respective output voltage during each mode can be calculated as,

$$V_{out} = V_{p1} + V_{p2} + V_{p3} = 7V_{in} \quad (21)$$

$$V_{out} = -(V_{n1} + V_{n2} + V_{n3}) = -7V_{in} \quad (22)$$

In summary, the resultant output voltage wave form is obtained by plotting all the output voltages during every respective mode.

III. Calculation of Losses

Phase deposition pulse width modulation (PD-PWM) is a technique used in multilevel inverters, particularly cascaded H-bridge inverters, to generate switching pulses for controlling the output voltage. It involves positioning carrier waves in the same phase, both above and below the zero reference line, to achieve lower harmonic distortion and reduced switching losses.

For the improved PDPWM method for the hybrid MMC, the circulating current harmonics cancellation PDPWM scheme and output voltage harmonics minimization PDPWM scheme are compared in the simulation and experiment. When the circulating current harmonics cancellation PDPWM scheme is applied, the equivalent switching frequency of the output voltage is 2fpd,hb (fpd,hb is the carrier frequency of HBSMs for PDPWM), the high frequency harmonics caused by modulation in the circulating current are cancelled. When the output voltage harmonics minimize PDPWM scheme is applied, the equivalent switching frequency of the output voltage is 4fpd,hb, but the circulating current contains high frequency harmonics caused by modulation. It can be concluded that the output voltage harmonics minimize PDPWM scheme has better output voltage harmonic characteristics than the circulating current harmonics cancellation PDPWM scheme.

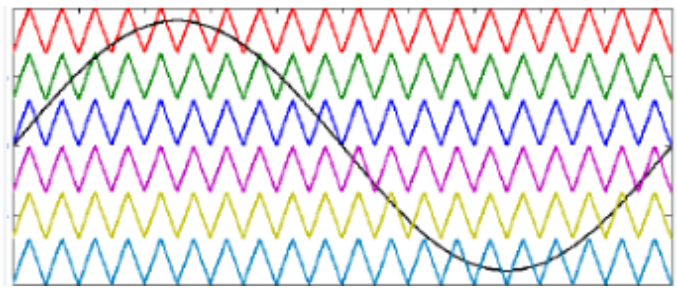

Fig. 5 Phase Disposition PWM

ISSN 2454-9940
www.ijasem.org
Vol 19, Issue 2, 2025

However, the circulating current harmonics cancellation PDPWM scheme has better circulating current harmonic characteristics than the output voltage harmonics minimize PDPWM scheme. Therefore, the output voltage harmonics minimize PDPWM scheme is a better scheme in the medium voltage applications with a small amount of SMs in each arm due to better output voltage harmonic characteristics. The circulating current harmonics cancellation PDPWM scheme is a better scheme in high voltage applications such as HVDC with a large amount of SMs in each arm due to better circulating current harmonic characteristics.

The simulation of PD PWM for optimizing the switching angles in multilevel inverters has provided insightful results, particularly in terms of Total Harmonic Distortion (THD) minimization. The algorithm's performance was evaluated over 100 iterations, as depicted in the provided THD vs. Iterations graph in fig.5. THD Minimization: The primary objective of PD PWM was to minimize THD by optimizing the switching angles of the multilevel inverter. Throughout the iterations, the algorithm demonstrated a significant ability to reduce the THD, with the best THD values fluctuating between 1.0% and 5.0% during the optimization process. This shows the algorithm's capability to explore the solution space effectively and achieve better results in subsequent iterations. In the early iterations, the THD values started relatively high but quickly began to drop, as the algorithm searched for more optimal switching angles. By the mid-iterations (around the 40th iteration), the algorithm was consistently finding lower THD values, with occasional jumps due to the exploratory nature of the Levy flight mechanism used by the Cuckoo Search Algorithm. Towards the end, the algorithm converged to better solutions, achieving a THD as low as 1.0%, demonstrating the efficacy of PD PWM in finding near-optimal switching angles. Optimization Performance: The Levy flight mechanism enabled the PD PWM to make both large exploratory jumps and smaller adjustments in the solution space. This allowed the algorithm to avoid local minima and find globally optimal or near-optimal solutions. The variation in THD across iterations shows that the algorithm was not prematurely converging and was instead continuously exploring the solution space. he best solutions were consistently selected, and in cases where the THD was improved, the algorithm replaced the older nests with the new solutions. The periodic discovery process (with a discovery probability of 25%) ensured that the algorithm did not get stuck in local optima, contributing to improved performance. Convergence Behavior:

The graph shows that PD PWM maintained a balanced exploration-exploitation trade-off throughout the simulation. While the THD values fluctuated during the iterations due to the stochastic nature of the algorithm, there was a clear trend of improvement as the iterations progressed. Around the 80th iteration, the algorithm appeared to stabilize, with smaller variations in THD values, indicating convergence towards an optimal solution. Comparison with Initial Conditions: The initial random values for switching angles resulted in relatively high THD values at the start, indicating poor power quality. However, the PD PWM successfully optimized these switching angles, reducing the THD significantly by up to 80% in some cases. This improvement highlights the potential of PD PWM to optimize the control parameters of multilevel inverters effectively. Practical Implications: Minimizing THD is crucial for improving the power quality in multilevel inverters, particularly in renewable energy systems where harmonic distortion can affect the efficiency and reliability of the entire system. The results demonstrate that PD PWM can be applied effectively in real-world applications to enhance the performance of multilevel inverters, reduce harmonic distortion, and ensure higher efficiency in energy conversion systems.

IV RESULTS

For a novel topological study to be developed, it must be properly validated. Thus, the reader is introduced to the suggested inverter's performance evaluation effort in this part. Finally, this part presents simulation-based responses of a suggested 15-L inverter unit, with experimental findings following.

An MLI is expected to produce equal stairs in its output so that the harmonic can be reduced as much as possible. In Fig. 7, the three-phase line-voltages, phase voltages and line currents of the proposed 15-L inverter are illustrated with and without filter components in steady-state condition. Generally, the quality of delivered power is measured in terms of the harmonic components appeared within output voltage and current waveforms. Hence, the corresponding THDs of the line voltages considering filtered and non-filtered cases are shown in Fig. 12.

INTERNATIONAL JOURNAL OF APPLIED SCIENCE ENGINEERING AND MANAGEMENT
ISSN 2454-9940
www.ijasem.org
Vol 19, Issue 2, 2025

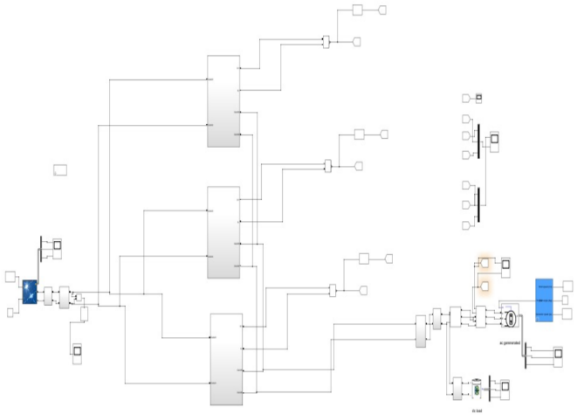

Fig.6 Simulation model

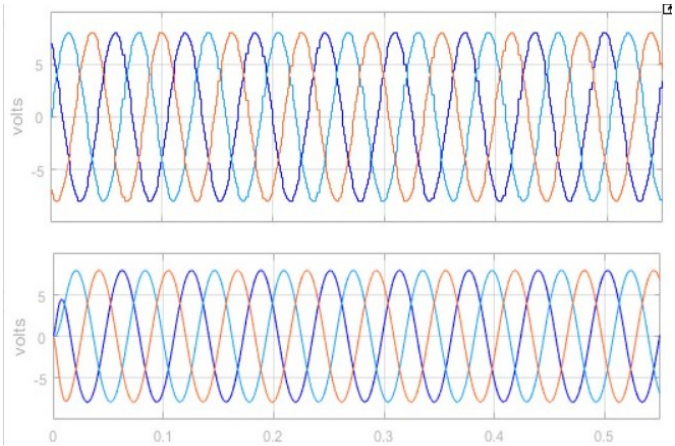

Fig. 7 15L voltage and filter voltage

Figure 7(b) displays the sin wave following LC filtering, whereas Figure 7(a) displays the 15 level voltage waveform produced by the proposed three phase multilevel inverter.

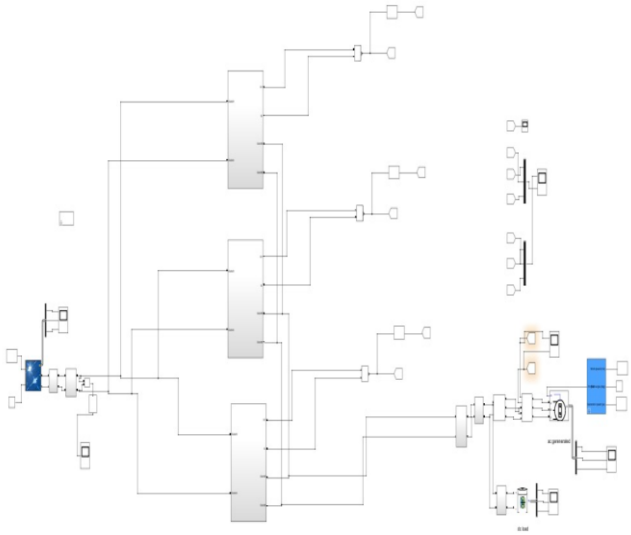

Fig.8 Simulation model with PD PWM

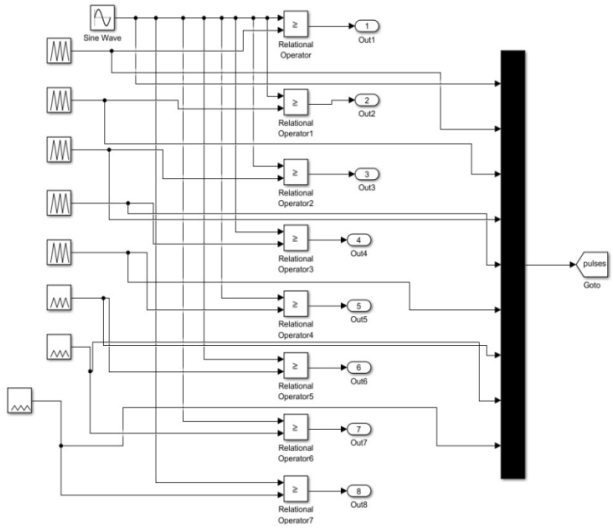

Fig. 9 PD PWM

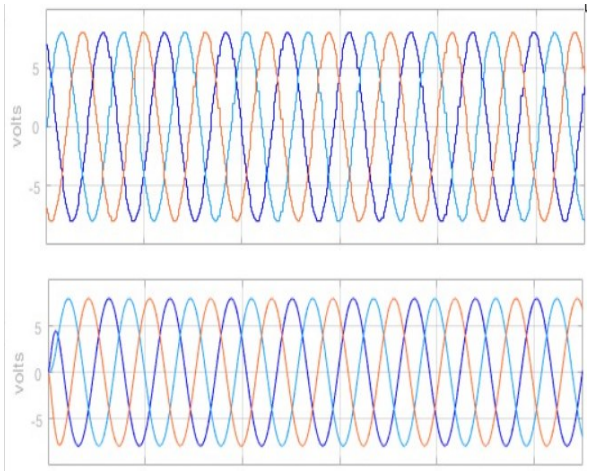

Fig. 10 Output waveform

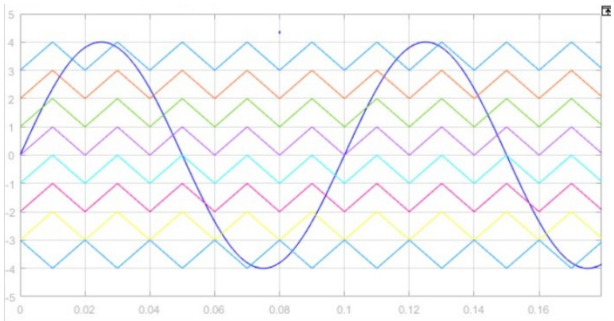

Fig. 11 PWM wave form

In this section, an overall comparative analysis is performed to ensure the superiority of the proposed inverter over the existing, which is summarized in Table V. The left half of Table V represents a numerical comparison between the proposed inverter and some existing inverters in terms of number of dc source (Ndc), number of switch (Nsw), number of diode (Nd), number driver circuit (Ndr), number of

capacitor (Nc), MVS, number of active switch rated with MVS, and TSV for a given level output. Since various topologies generate different level output equipping different

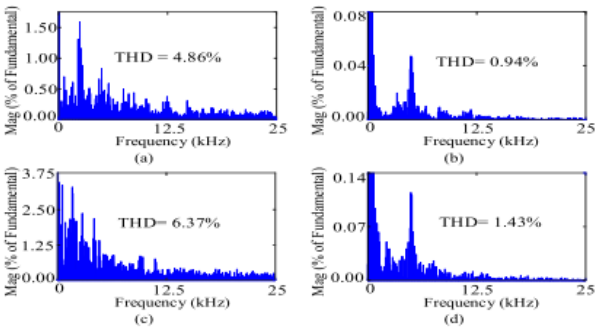

Fig.12 THD

number of components, it will be worth if comparison is performed in the form of per-level ratio. Therefore, a fair comparison is obtained and shown in the right half of Table V, where the per-level ratios for all the corresponding components are demonstrated.

V CONCLUSION

The application of PD PWM to optimize switching angles for multilevel inverters has proven to be highly effective in minimizing Total Harmonic Distortion (THD). Through iterative optimization and the use of Levy flights for exploration, the algorithm successfully reduced THD from higher initial values to as low as 1.0%, improving the overall power quality of the inverter's output. The minimized THD not only enhances power quality but also increases the efficiency and reliability of renewable energy systems where multilevel inverters are widely used. The study illustrates that PD PWM can be a powerful tool in real world applications, particularly for renewable energy systems such as photovoltaic (PV) and wind power systems. By optimizing the inverter's switching angles, PD PWM helps reduce harmonic distortion, improving the system's overall performance and energy conversion efficiency.

REFERENCES

[1] M. Halim Mondol, S. Prokash Biswas, M. Faruk Kibria, M. Rabiul Islam, M. Ashib Rahman, and K. M. Muttaqi, "A new integrated multilevel inverter topology for renewable energy transformation," in *Proc. IEEE Ind. Appl. Soc. Annu. Meeting*, 2021, pp. 1–6.

[2] S. Peddapati and V. S. Prasadarao K, "A new fault-tolerant multilevel inverter structure with reduced device count and low total standing voltage," *IEEE Trans. Power Electron.*, vol. 37, no. 7, pp. 8333–8344, Jul. 2022.

[3] M. H. Mondol, M. R. Tür, S. P. Biswas, M. K. Hosain, S. Shuvo, and E. Hossain, "Compact three phase multilevel inverter for low and medium power photovoltaic systems," *IEEE Access*, vol. 8, pp. 60824–60837, 2020.

[4] T.RoyandP.K.Sadhu,"Astep-upmultilevelinvertertopologyusingnovel switchedcapacitorconverterswithreducedcomponents,"*IEEETrans.Ind. Electron.*, vol. 68, no. 1, pp. 236–247, Jan. 2021.

[5] M. H. Mondol, M. S. Uddin, E. Hossain, and S. P. Biswas, "A compact and cost efficient multiconverter for multipurpose applications," *IEEE Access*, vol. 8, pp. 86810–86823, 2020.

[6] P. Omer, J. Kumar, and B. S. Surjan, "A review on reduced switch count multilevel inverter topologies," *IEEE Access*, vol. 8, pp. 22281–22302, 2020.

[7] M. H. Mondol, S. P. Biswas, and M. K. Hosain, "A new magnetic linked three-phase multilevel inverter with reduced number of switches and balanced DC sources," *Elect. Eng.*, vol. 104, pp. 449–461, Apr. 2022.

[8] C. Terbrack, J. Stöttner, and C. Endisch, "Design and validation of the parallel enhanced com-mutation integrated nested multilevel inverter topology,"*IEEETrans.PowerElectron.*,vol.37,no.12,pp. 15163–15174, Dec. 2022, doi: 10.1109/TPEL.2022.3183859.

[9] P. K. Chamarthi, A. Al-Durra, T. H. M. EL-Fouly, and K. A. Jaafari, "A novel three-phase transformerless cascaded multilevel inverter topology for grid-connected solar PV applications," *IEEE Trans. Ind. Appl.*, vol. 57, no. 3, pp. 2285–2297, May/Jun. 2021.

[10] A. Salem, H. Van Khang, K. G. Robbersmyr, M. Norambuena, and J. Rodriguez, "Novel three-phase multilevel inverter with reduced components for low- and high-voltage applications," *IEEE Trans. Ind. Electron.*, vol. 68, no. 7, pp. 5978–5989, Jul. 2021.

[11] A. Taghvaie, J. Adabi, and M. Rezanejad, "A self-balanced step-up multilevel inverter based on switched-capacitor structure," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 199–209, Jan. 2018.

[12] J. S. Mohamed Ali and V. Krishnasamy, "Compact switched capacitor multilevel inverter (CSCMLI) with self-voltage balancing and boosting ability," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4009–4013, May 2019.

[13] M. Saeedian, M. E. Adabi, S. M. Hosseini, J. Adabi, and E. Pouresmaeil, "A novel step-up single source multilevel inverter: Topology, operating principle, and modulation," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3269–3282, Apr. 2019.

[14] M. D. Siddique, S. Mekhilef, S. Padmanaban, M. A. Memon, and C. Kumar, "Single-phase step-up switched-capacitor-based multilevel inverter topology with SHEPWM," *IEEE Trans. Ind. Appl.*, vol. 57, no. 3, pp. 3107–3119, May/Jun. 2021.

[15] M. JagabarSathik, N. Sandeep, D. Almakhles, and F. Blaabjerg, "Cross connected compact switched-capacitor multilevel inverter (C3-SCMLI) topology with reduced switch count," *IEEE Trans. Circuits Syst. II: Exp. Brief.*, vol. 67, no. 12, pp. 3287–3291, Dec. 2020.

[16] K.P.Panda,P.R.Bana,andG.Panda,"Aswitched-capacitorself-balanced high-gain multilevel inverter employing a single DC

source," *IEEE Trans. Circuits Syst. II: Exp. Brief.*, vol. 67, no. 12, pp. 3192–3196, Dec. 2020.

[17] M. F. Talooki, M. Rezanejad, R. Khosravi, and E. Samadaei, "A novel high step-up switched-capacitor multilevel inverter with self-voltage balancing," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 4352–4359, Apr. 2021.

[18] Y.Wang,Y.Yuan,G.Li,Y.Ye,K.Wang,andJ.Liang,"AT-typeswitchedcapacitor multilevel inverter with low voltage stress and self-balancing," *IEEETrans.CircuitsSyst.I:RegularPapers*,vol.68,no.5,pp. 2257–2270, May 2021.

[19] M. Farhangi, R. Barzegarkhoo, R. P. Aguilera, S. S. Lee, D. D.-C. Lu, and Y. P. Siwakoti, "A single-source single-stage switched-boost multilevel inverter: Operation, topological extensions, and experimental validation," *IEEE Trans. Power Electron.*, vol. 37, no. 9, pp. 11258–11271, Sep. 2022, doi: 10.1109/TPEL.2022.3163762.

[20] K. P. Panda, P. R. Bana, O. Kiselychnyk, J. Wang, and G. Panda, "A singlesource switched-capacitor-based step-up multilevel inverter with reduced components," *IEEE Trans. Ind. Appl.*, vol. 57, no. 4, pp. 3801–3811, Jul./Aug. 2021.

[21] M. A. Hosseinzadeh, M. Sarebanzadeh, C. F. Garcia, E. Babaei, and J. Rodriguez,"Anasymmetricswitched-capacitormulticellinverterwithlow number of DC source and voltage stress for renewable energy sources," *IEEE Access*, vol. 10, pp. 30513–30525, 2022.

[22] R. Sun, X. Wang, and Y. Ye, "Seventeen-level inverter based on switchedcapacitor and flying-capacitor-fed T-type unit," *IEEE Access*, vol. 10, pp. 33561–33570, 2022.

[23] K. P. Panda, P. R. Bana, R. T. Naayagi, and G. Panda, "A dual-source self-balanced switched-capacitor reduced switch multilevel inverter with extending ability," *IEEE Access*, vol. 10, pp. 61441–61450, 2022.

[24] R.Barzegarkhoo,M.Forouzesh,S.S.Lee,F.Blaabjerg,andY.P.Siwakoti, "Switched-capacitor multilevel inverters: A comprehensive review," *IEEE Trans. Power Electron.*, vol. 37, no. 9, pp. 11209–11243, Sep. 2022, doi: 10.1109/TPEL.2022.3164508.

[25] E.Samadaei,A.Sheikholeslami,S.A.Gholamian,andJ.Adabi,"As quare T-type (ST-Type) module for asymmetrical multilevel inverters," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 987–996, Feb. 2018.

[26] S. S. Lee, M. Sidorov, N. R. N. Idris, and Y. E. Heng, "A symmetrical cascaded compact-module multilevel inverter (CCM-MLI) with pulsewidth modulation," *IEEE Trans. Ind. Electron.*, vol. 65, no. 6, pp. 4631–4639, Jun. 2018.

[27] E.Samadaei,M.Kaviani,andK.Bertilsson,"A13-levelsmodule(K-Type) with two DC sources for multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 66, no. 7, pp. 5186–5196, Jul. 2019.

[28] M.Sarebanzadeh,M.A.Hosseinzadeh,C.Garcia,E.Babaei,S.Islam ,and J.Rodriguez,"Reducedswitchmultilevelinvertertopologiesforren ewable energy sources," *IEEE Access*, vol. 9, pp. 120580–120595, 2021.

[29] M. D. Siddique, S. Mekhilef, N. M. Shah, A. Sarwar, and M. A. Memon, "A new single-phase cascaded multilevel inverter topology with reduced number of switches and voltage stress," *Int. Trans. Elect. Energy Syst.*, vol. 30, pp. 1–21, 2020.