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Design and Implementation of a 64-bit ALU Using Vedic Mathematics

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Abstract: In the era of high-performance and power-sensitive applications, reducing energy consumption without compromising processing speed has emerged as a major design challenge in system-on-chip (SoC) architectures. This research proposes a novel 64-bit Arithmetic Logic Unit (ALU) that leverages Vedic Mathematics for computational efficiency and low-power Very Large-Scale Integration (VLSI) techniques for minimizing energy dissipation. The key innovation lies in the integration of the Urdhva Tiryakbhyam Sutra—an ancient Vedic multiplication technique—within the ALU's arithmetic unit to accelerate multiplication operations and reduce computational latency. The design also incorporates ripple carry adders, Kogge-Stone adders, subtractors, logical units, comparators, and shifters, all optimized for low static and dynamic power consumption. Power gating techniques are applied at the architectural level to selectively deactivate unused components, reducing leakage currents and conserving energy during idle states.

I. INTRODUCTION:

The evolution of integrated circuits and system-on-chip (SoC) technology has significantly transformed the digital design landscape, ushering in a new era of compact, fast, and energy-efficient computing systems. Among the essential components of any computing device, the Arithmetic Logic Unit (ALU) plays a central role in performing mathematical, logical, and decision-based operations. With the increasing demand for portable electronics, edge computing, artificial intelligence (AI), and IoT-based systems, there is a growing necessity to design ALUs that are not only fast but also highly energy-efficient.

Power consumption in digital systems is broadly categorized into dynamic and static power. While dynamic power is consumed during switching activities, static power, caused by leakage currents, becomes more

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Vol 19, Issue 2, 2025

significant as transistor sizes shrink in advanced fabrication nodes. Consequently, reducing static power has become a pivotal aspect of modern VLSI design. This necessitates innovative techniques that optimize performance without compromising power efficiency.

In parallel, the revival of ancient computational methods, such as Vedic Mathematics, has provided unconventional yet highly effective techniques to enhance arithmetic operation speed. Specifically, the Urdhva Tiryakbhyam (vertical and crosswise) Sutra offers a parallel and scalable approach to binary multiplication, reducing computational complexity and delay. When integrated into digital circuit design, such techniques complement conventional hardware approaches by providing faster and more compact arithmetic logic units.

This paper explores the integration of Vedic arithmetic techniques and low-power design methodologies to create a high-performance 64-bit ALU. The proposed architecture not only accelerates key arithmetic operations but also implements power gating strategies at the architectural level to curtail static power loss. Developed using Verilog HDL and tested on FPGA platforms, the proposed ALU is rigorously evaluated for performance, area, and energy metrics. The goal is to demonstrate the viability of combining traditional computation with modern design innovations to meet the growing demands of next-generation digital systems.

II. SCOPE OF THE PROJECT:

The Scope of the Project 64-bit ALU using Vedic Mathematics has a wide scope in modern computing applications due to its high-speed performance, reduced power consumption, and optimized hardware design. The project is designed to improve multiplication efficiency by implementing the Urdhva Tiryakbhyam Sutra, making it highly suitable for real-time and high-performance computing. The ALU's adaptability makes it viable for integration in embedded systems, edge AI devices, and IoT applications. Its modular design supports future expansion, allowing seamless upgrades to higher-bit architectures.

The low-power characteristics also position it as a valuable component for battery-operated systems where energy efficiency is critical. Write detail about proposed system

Moreover, its applicability extends beyond conventional computing into sectors such as autonomous systems, robotics, and wearable technology. These areas demand compact yet powerful computational units, making this ALU a key enabler in next-generation, intelligent electronic platforms.

ISSN 2454-9940
www.ijasem.org
Vol 19, Issue 2, 2025

III. PROPOSED SYSTEM

The proposed system introduces a high-speed, low-power 64-bit Arithmetic Logic Unit (ALU) that integrates Vedic Mathematics for multiplication operations alongside traditional arithmetic units. The architectural design leverages modularity, parallelism, and power-efficient control mechanisms to ensure optimal performance for real-time applications. The key modules within the ALU are coordinated by a control unit and a 4:1 multiplexer, enabling dynamic selection of arithmetic functions based on system requirements. Each module is described in detail below.

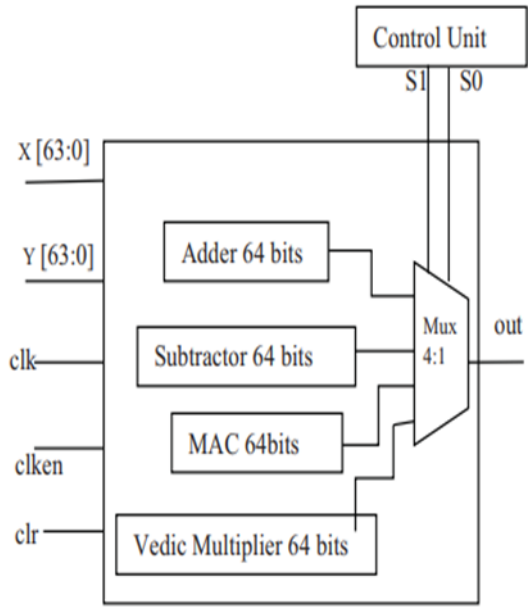

Fig1: Block diagram of proposed system

Input Operands: -The architecture accepts two primary 64-bit inputs, denoted as X [63:0] and Y [63:0], which are simultaneously fed into all computational units. These inputs represent the operands for all supported operations—addition, subtraction, multiplication, and MAC (Multiply and Accumulate). The parallel input configuration enables all sub-modules to be computation-ready, thereby reducing switching latency during operation selection.

Clocking and Control Signals: -The system is driven by three essential control signals: clk (clock), clken (clock enable), and clr (clear). The clock signal ensures synchronized execution across all components. The clock enable signal allows conditional activation of processing modules, thereby contributing to reduced dynamic power consumption. The clear signal initializes or resets the ALU, clearing intermediate data and preparing the system for the next operation cycle.

Arithmetic Units:- Four primary arithmetic units are embedded in the system to perform core computational functions:

a. The 64-bit Adder performs binary addition using optimized fast adders. It is designed for minimal propagation

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www.ijasem.org
Vol 19, Issue 2, 2025

delay and efficient logic utilization.

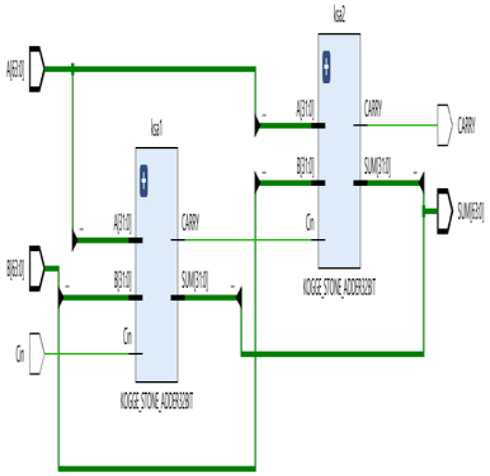

Fig 2:64-bit adder schematic

b. The 64-bit Subtractor executes subtraction using two's complement logic, sharing much of the adder's architecture to maximize resource efficiency.

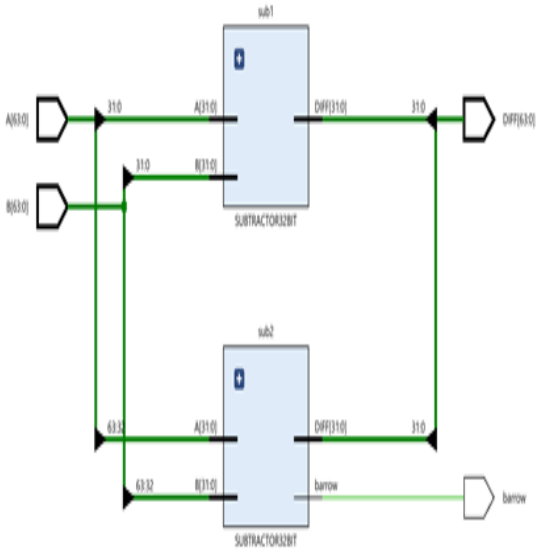

Fig 3:64-bit subtractor schematic

c. The 64-bit MAC Unit (Multiply and Accumulate) is tailored for high-performance DSP applications. It computes the product of X and Y and adds the result to an accumulator register, enhancing throughput in repetitive computation scenarios.

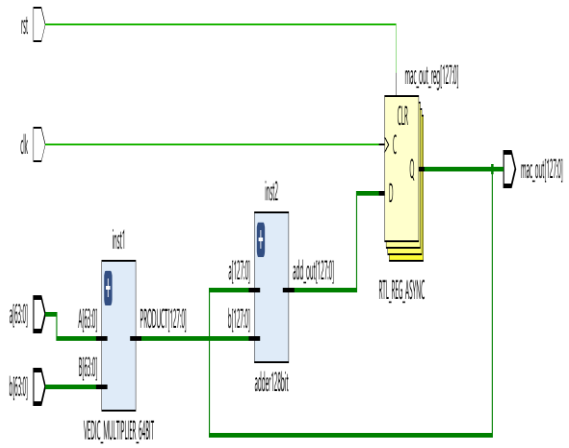

Fig 4:64-bit MAC schematic

d. The 64-bit Vedic Multiplier employs the Urdhva Tiryakbhyam sutra from Vedic Mathematics. This multiplier enables parallel partial product generation, significantly reducing the multiplication time and power dissipation compared to conventional multipliers.

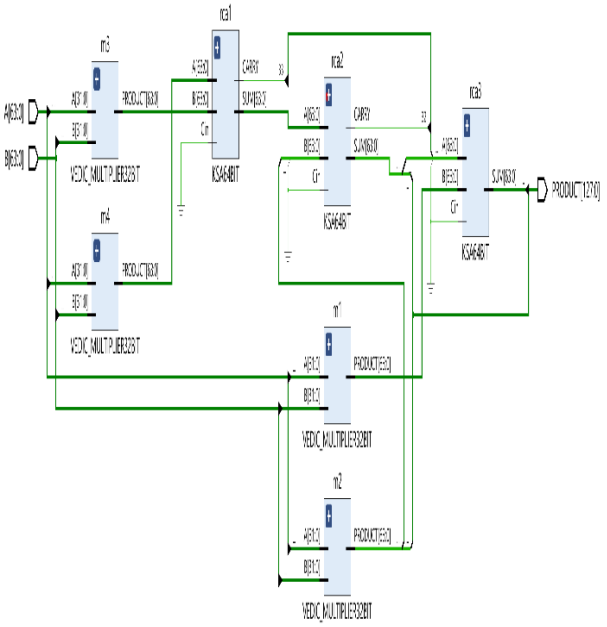

Fig 5:64-bit Vedic multiplier schematic

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ISSN 2454-9940
www.ijasem.org
Vol 19, Issue 2, 2025

Multiplexer and Control Unit:- The 4:1 Multiplexer acts as a selector that chooses one of the four arithmetic results based on the control signals S1 and S0 provided by the Control Unit. The control unit governs the overall operation of the ALU by determining which arithmetic function is executed at any given time. This configuration ensures that only the required module drives the output, allowing the rest to remain in an idle state, conserving energy.

System Output: -The selected result from the multiplexer is routed to the ALU's output terminal, labeled out. This output represents the final computed result of the selected operation, ready to be transferred to the next stage of the system or stored for further processing.

to avoid or mitigate the impact of an accident. These systems enhance overall safety by reducing the likelihood of human error, contributing to fewer road accidents and safer driving conditions.

Output based on selection line

S1	S0	Selected Operation	Output Source
0	0	Addition	64-bit Adder Output
0	1	Subtraction	64-bit Subtractor Output
1	0	MAC Operation	64-bit MAC Output
1	1	Vedic Multiplication	64-bit Vedic Multiplier

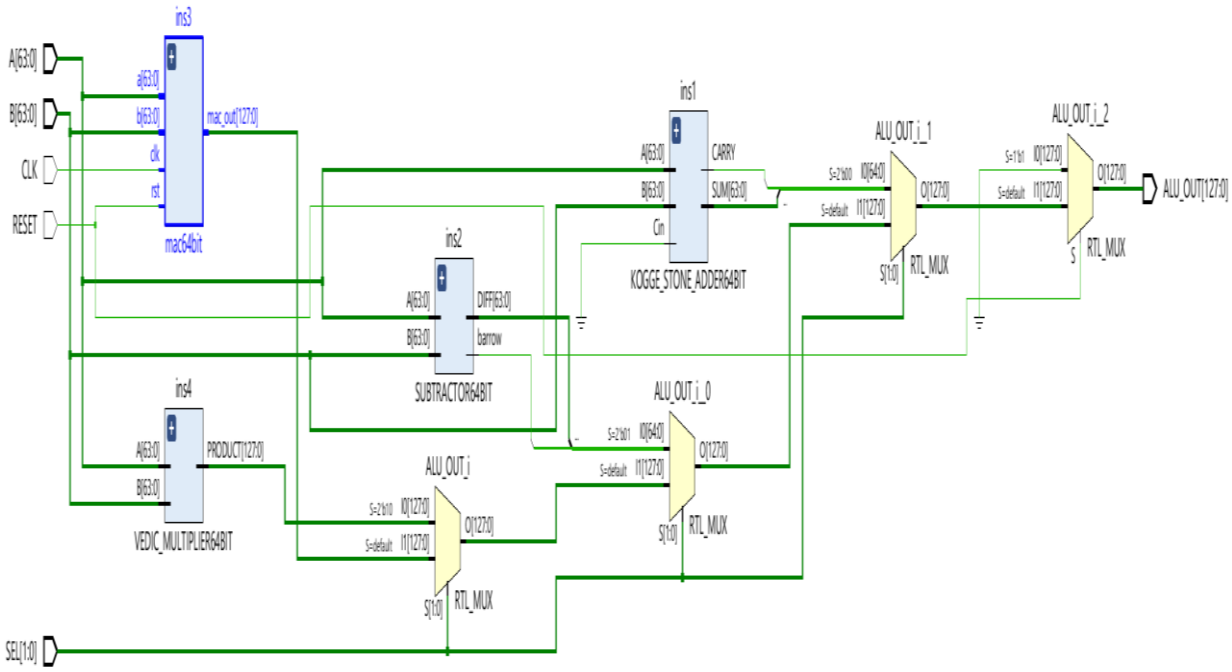

Fig 6: Proposed ALU Schematic

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ISSN 2454-9940
www.ijasem.org
Vol 19, Issue 2, 2025

IV. RESULT: -

To validate the functional correctness and performance of the proposed 64-bit ALU based on Vedic Mathematics, a testbench was developed using Verilog HDL and simulated using the Xilinx ISE 14.7 tool. The waveform output generated during simulation confirms that the ALU operates accurately according to the selected control signals. The analysis of one such simulation instance is discussed below.

Test Case Overview: -

In the selected test scenario:

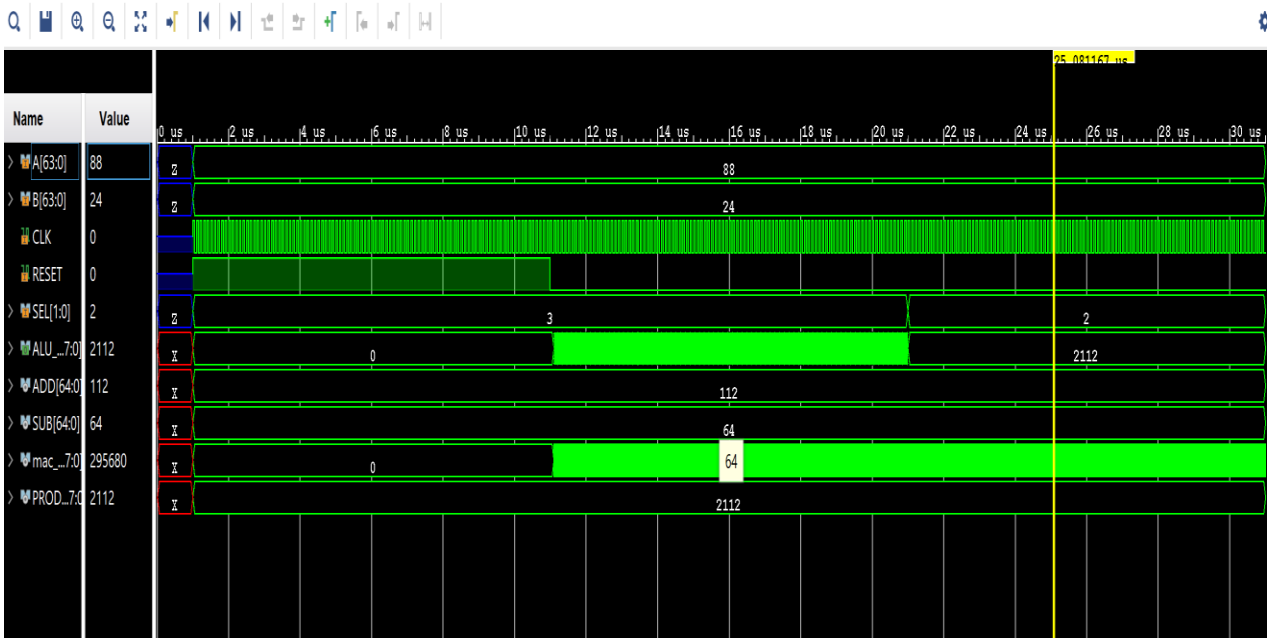

Fig 7: Simulation output of the test

Operand A is given as 88 (64-bit input).

Operand B is given as 24 (64-bit input).

The SEL signal is set to 10 (binary for 2), which corresponds to the multiplication operation in the ALU's selection logic.

The multiplication operation leverages the Vedic Urdhva-Tiryakbhyam Sutra, which allows efficient parallelism and reduces the complexity typically associated with conventional multiplication algorithms. This Vedic multiplier is deeply integrated into the ALU data path to handle high-speed 64-bit operations.

Simulation Output

The waveform shows the following outputs:

ADD[64:0] = 112 → Verifies that addition logic (A + B) = 88 + 24 = 112

SUB[64:0] = 64 → Verifies that subtraction logic (A - B) = 88 - 24 = 64

PRODUCT = 2112 → Represents the output of the Vedic multiplier for A × B = 88 × 24 = 2112.

mac_result = 295680 → Indicates the output of a MAC (Multiply-Accumulate)

ISSN 2454-9940
www.ijasem.org
Vol 19, Issue 2, 2025

operation, which may represent (A × B) + C, where C is a predefined or stored value (not shown in this cycle)

ALU Output Selection

Since SEL = 2, the ALU correctly routes the multiplication output (2112) to the primary output line ALU_OUT, confirming the successful operation of the selection multiplexer and functional modules.

V. CONCLUSION

Vedic Mathematics concepts for various mathematical computations are proved to be efficient as compared to conventional methods. Many researchers have proposed computational units based on Vedic Mathematics for various signal processing applications and these designs are proved to be efficient ones. The proposed Vedic Mathematics based ALU uses Urdhva-Tiryakbyham Sutra implementation of multiplication, logical functions and addition respectively. The proposed ALU architecture would find application in various signal processing areas. In future these structures will be used to upgrade obsolete integrated circuits reduces hardware circuit board changes, increases productivity, and ensures that the operational constraints are met.

VI. SSFUTURE SCOPE

The 64-bit Vedic Mathematics-based ALU design presents strong potential for further development. In the future, it can be implemented on real hardware like FPGA or ASIC for practical verification. The design can be enhanced to support floating-point operations and integrated into modern processor architectures such as RISC-V or ARM. Optimization techniques like pipelining and power reduction can make it suitable for high-speed, low-power applications. Additionally, it holds promise in fields like cryptography, AI, and education, where fast arithmetic and efficient computation are essential. Developing a dedicated Vedic instruction set could further extend its applications in specialized processors. Advanced

1. Hardware Implementation:

Deploying the design on FPGA or converting it into ASIC for real-time hardware testing and validation.

2. Floating-Point Extension:

Expanding the ALU to support IEEE-754 floating-point operations for applications in DSP and scientific computing.

3. Processor Integration:

Integrating the ALU with RISC-V or ARM processors to evaluate its efficiency in modern embedded systems.

4. Power and Speed Optimization:

ISSN 2454-9940
www.ijasem.org
Vol 19, Issue 2, 2025

Applying pipelining, clock gating, or low-power techniques to improve performance and energy efficiency.

5. Applications in AI and Cryptography:

Utilizing the ALU for fast, large-number computations in cryptographic systems and AI accelerators.

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