ISSN: 2454-9940

INTERNATIONAL JOURNAL OF APPLIED SCIENCE ENGINEERING AND MANAGEMENT

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INTERNATIONAL JOURNAL OF APPLIED SCIENCE ENGINEERING AND MANAGEMENT
ISSN 2454-9940
www.ijasem.org
Vol 19, Issue 2, 2025

Design of Low Power High Performance 2-4 and 4-16 Mixed Logic Line Decoders

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Abstract –

This brief introduces a mixed-logic design method for line decoders, combining transmission gate logic, pass transistor dual-value logic, and static complementary metal-oxide semiconductor (CMOS). Two novel topologies are presented for the 2–4 decoder: a 14-transistor topology aiming on minimizing transistor count and power dissipation and a 15-transistor topology aiming on high power-delay performance. Both normal and inverting decoders are implemented in each case, yielding a total of four new designs. Furthermore, four new 4–16 decoders are designed by using mixed-logic 2–4 pre-decoders combined with standard CMOS post decoder. All proposed decoders have full-swinging capability and reduced transistor count compared to their conventional CMOS counterparts. Finally, a variety of comparative spice simulations at 32 nm shows that the proposed circuits present a significant improvement in power and delay, outperforming CMOS in almost all cases.

Keywords – Line decoder, mixed-logic, power-delay optimization.

I. INTRODUCTION

The present invention relates to a reversible logic gates and implementation of digital decoders using reversible logic gates. The encoded input information need be preserved at the output in computational tasks pertaining to digital signal processing, communication, computer graphics, and cryptography applications. The conventional computing circuits are irreversible i.e. the input bits are lost when the output is generated. This information loss during computation culminates into increased power consumption. According to Landauer, for each bit of information that is lost during the computation generates KTln2 Joules of heat energy where K and T respectively represent Boltzmann's constant and absolute temperature. The information loss becomes more frequent for high-speed systems thereby leading to increased heat energy. C. Bennett demonstrated that power dissipation in can be significantly reduced the same operation is done reversibly. The reversible logic allows the circuit to go back at any point of time therefore no bit of information is actually lost and the amount of heat generated is negligible. In digital design, decoders find extensive usage - in addressing a particular location for read/write operation in memory cells, in I/O processors for connecting a memory chip to the CPU; and also, in Analog to Digital (ADC) and Digital to Analog Converters (DAC) which are used in various different stages of a communication system. This paper therefore addresses the design of reversible decoders. The literature survey on reversible decoders shows that the focus is on either developing topology based on available reversible gates or present an altogether new gate for the said purpose.

Objectives Of the Project:

The main objective is to design a reversible logic gates and implementation of a digital decoders using reversible logic gates.

Other objectives are given below:

i) To design both non-reversible and reversible versions of decoders along with analytical evaluation of the design complexities both in terms of delay and resource requirements.

ii) To optimize the final garbage outputs, constant inputs optimizing techniques are also implemented.

iii) we present an efficient reversible implementation of decoders for all digital applications**.**

iv) The comparative results show that the proposed design is much better in terms of quantum cost, delay, hardware complexity and has significantly better scalability than the existing approach.

II. EXISTING METHOD

The Binary Decoder is another combinational logic circuit constructed from individual logic gates and is the exact opposite to that of an "Encoder" we looked at in the last tutorial. The name "Decoder" means to translate or decode coded information from one format into another, so a digital decoder transforms a set of digital input signals into an equivalent decimal code at its output. Binary Decoders are another type of Digital Logic device that has inputs of 2-bit, 3-bit or 4-bit codes depending upon the number of data input lines, so a decoder that has a set of two or more bits will be defined as having an *n*-bit code, and therefore it will be possible to represent 2^n possible values. Thus, a decoder generally decodes a binary value into a non-binary one by setting exactly one of its *n* outputs to logic "1". If a binary decoder receives n inputs (usually grouped as a single Binary or Boolean number) it activates one and only one of its 2^n outputs based on that input with all other outputs deactivated. A *Binary Decoder* converts coded inputs into coded outputs, where the input and output codes are different and decoders are available to "decode" either a Binary or BCD (8421 code) input pattern to typically a Decimal output code. Commonly available BCD-to-Decimal decoders include the TTL 7442 or the CMOS 4028. Generally, a decoders output code normally has more bits than its input code and practical "binary decoder" circuits include, 2-to-4, 3-to-8 and 4-to-16-line configurations. The existing method**,** decoders like of 2:4 and 3:8 decoders are designed by using conventional gates like and, not, xor etc. using the Boolean expressions.

III. PROPOSED METHOD

Reversible gates have equal number of inputs and outputs; and each of these input output combinations is unique. An n input n output reversible gate is represented as n x n gate. The inputs which assume value '0' or '1' during the operation are termed as constant inputs. On the other hand, the number of outputs introduced for maintaining reversibility is called garbage outputs. Some of the most widely and commonly used reversible gates are Feynman Gate (FG), Fredkin Gate (FRG), Peres gate (PG) and Toffoli gate (TG). Out of these gates Feynman gate is a 2 x 2 gate while Peres, Toffoli and Fredkin gates belong to 3 x 3 gates. The cost of reversible gate is given in terms of number of primitive reversible gates

needed to realize the circuit. The development in the field of nanometer technology leads to minimize the power consumption of logic circuits. Reversible logic design has been one of the promising technologies gaining greater interest due to less dissipation of heat and low power consumption. In the digital design, the multiplexer is a widely used process. Reversible logic plays an extensively important role in low power computing as it recovers from bit loss through unique mapping between input and output vectors. Power consumption is an important issue in modern day VLSI designs. The development in the field of nanometer technology leads to minimize the power consumption of logic circuits. Reversible logic design has been one of the promising technologies gaining greater interest due to less dissipation of heat and low power consumption. In the digital design, the decoder is a widely used process. So, the reversible logic gates and reversible circuits for realizing decoders like of 2:4,3:8,4:16 reversible decoder using reversible logic gates is proposed. The proposed design leads to the reduction of power consumption compared with conventional logic circuits.

IV. DECODER

In digital electronics, a binary decoder is a combinational logic circuit that converts a binary integer value to an associated pattern of output bits. They are used in a wide variety of applications, including data de-multiplexing, seven segment displays, and memory address decoding. There are several types of binary decoders, but in all cases a decoder is an electronic circuit with multiple data inputs and multiple outputs that converts every unique combination of data input states into a specific combination of output states. In addition to its data inputs, some decoders also have one or more "enable" inputs. When the enable input is negated (disabled), all decoder outputs are forced to their inactive states. Depending on its function, a binary decoder will convert binary information from n input signals to as many as 2^n unique output signals. Some decoders have less than 2^n output lines; in such cases, at least one output pattern will be repeated for different input values.

1-of-n decoder:

A 1-of-n binary decoder has n output bits, and the integer inputs bits serve as the "address" or bit number of the output bit that is to be activated. This type of decoder asserts exactly one of its n output bits, or none of them, for every unique combination of input bit states. Each output bit becomes active only when a specific, corresponding integer value is applied to the inputs.

1-to-2-line decoder:

A decoder is a circuit that changes a code into a set of signals. It is called a decoder because it does the reverse of encoding, but we will begin our study of encoders and decoders with decoders because they are simpler to design. A common type of decoder is the line decoder which takes an n-digit binary number and decodes it into 2^n data lines. The simplest is the 1-to-2 line decoder. The truth table is

A	D_1	D_0
0	0	1
1	1	0

I. Truth table 1 to 2 decoder

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ISSN 2454-9940
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A is the address and D is the dataline. D_0 is NOT A and D_1 is A. The circuit looks like

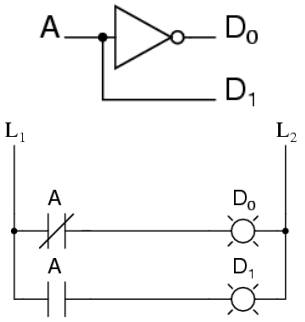

Fig.1: circuit diagram of 1 to 2 decoder

2-to-4 line decoder:

Only slightly more complex is the 2-to-4 line decoder. The truth table is

A_1	A_0	D_3	D_2	D_1	D_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

II. Truth table 2 to 4 decoder

Developed into a circuit it looks like

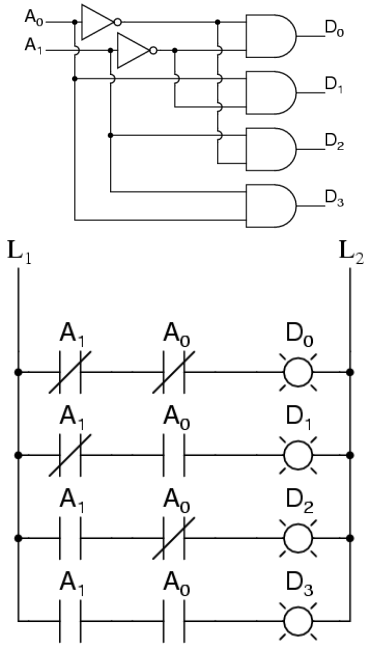

Fig.2: circuit diagram of 2 to 4 decoder

Larger line decoders can be designed in a similar fashion, but just like with the binary adder there is a way to make larger decoders by combining smaller decoders. An alternate circuit for the 2-to-4 line decoder is

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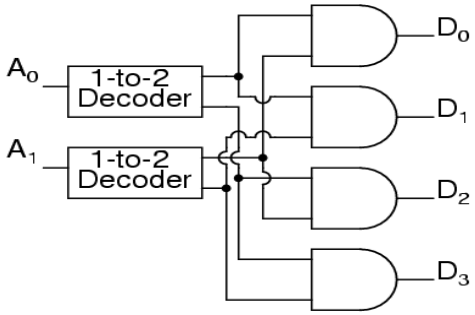

Fig.3: An alternate circuit for the 2-to-4 line decoder

Replacing the 1-to-2 Decoders with their circuits will show that both circuits are equivalent. In a similar fashion a 3-to-8 line decoder can be made from a 1-to-2 line decoder and a 2-to-4 line decoder, and a 4-to-16 line decoder can be made from two 2-to-4 line decoders. You might also consider making a 2-to-4 decoder ladder from 1-to-2 decoder ladders. If you do it might look something like this:

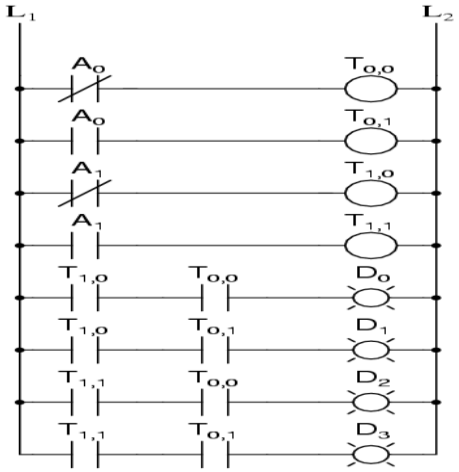

Fig.4: 2-to-4 decoder ladder from 1-to-2 decoder ladders

For some logic it may be required to build up logic like this. For an eight-bit adder we only know how to sum eight bits by summing one bit at a time. Usually, it is easier to design ladder logic from boolean equations or truth tables rather than design logic gates and then "translate" that into ladder logic.

V. SIMULATION RESULTS

The corresponding simulation results of the adders are shown below.

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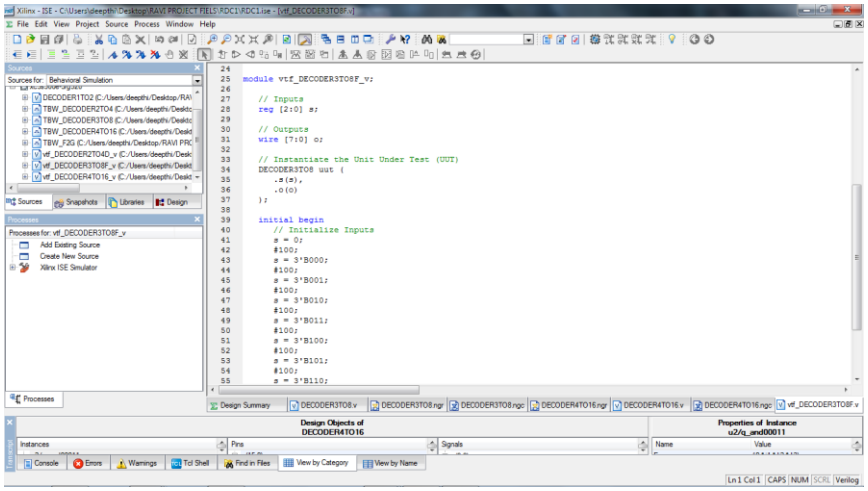

Fig.5: Test Bench for 3 to 8 Reversible Decoder

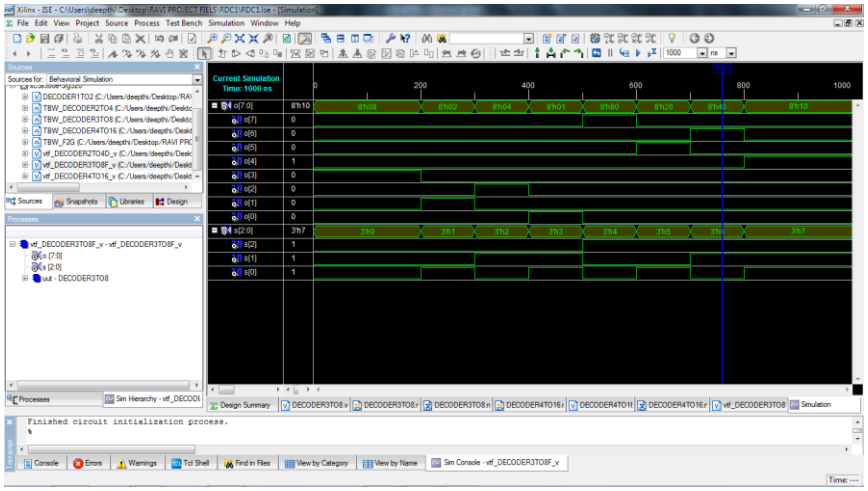

Fig.6: Simulated output for 3 to 8 Reversible Decoder

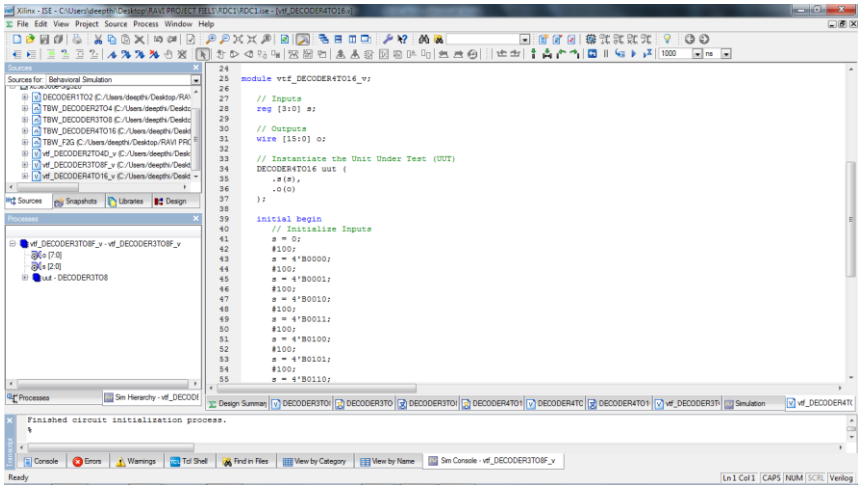

Fig.7: Test Bench for 4 to 16 Reversible Decoder

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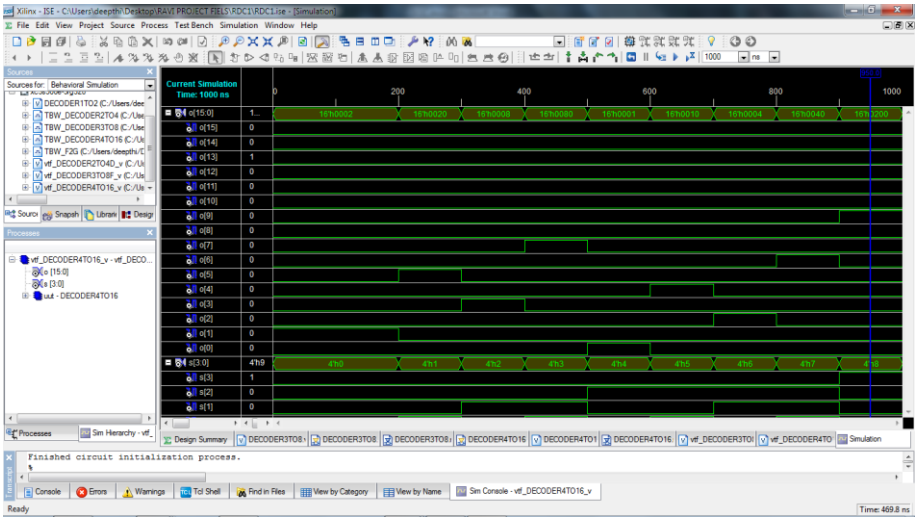

Fig.8: Simulated output for 4 to 16 Reversible Decoder

CONCLUSION

we presented the design methodologies of an n-to-2n reversible fault tolerant decoder, where n is the number of data bits. We proposed several lower bounds on the numbers of garbage outputs, constant inputs and quantum cost and proved that the proposed circuit has constructed with the optimum garbage outputs, constant inputs and quantum cost. In addition, we presented the designs of the individual gates of the decoder using MOS transistors in order to implement the circuit of the decoder with transistors. Simulations of the transistor implementation of the decoder showed that the proposed fault tolerant decoder works correctly. The comparative results proved that the proposed designs perform better than its counterpart. We also proved the efficiency and supremacy of the proposed scheme with several theoretical explanations. Proposed reversible fault tolerant decoders can be used in parallel circuits, multiple-symbol differential detection, network components and in digital signal processing etc.

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