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DESIGN AND ANALYSIS OF 4:1 MULTIPLEXER USING TRANSMISSION GATE AND GDI TECHNIQUES AT 16NM REGIME

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ABSTRACT

Nowadays, when it comes to downsizing, power efficiency and smaller die sizes are king. The multiplexer is an essential component of any digital infrastructure. Using this method, SOPs for many other kinds of circuits, including adders, sub tractors, and others, are possible to create. We examine the delay and power consumption of the multiplexer at several technology crossroads. The traditional AND, OR, and NAND gates of MOSFETs—made possible with 16nm technology—are implemented using the TG gate type. We examined the impact of variables such as process and supply voltage on the following metrics: delay, average power, power delay product, and energy-delay product; and we conducted sensitivity analyses on these variables. The less sophisticated node uses more power, but it's cramped. The quickest choice, however, is the simpler technology. If the supply voltage is reduced by 33% for 16 nm, the delay is increased by 209.46% and the power consumption is decreased by 90.82%; for 14 nm, the equivalent reductions are 193.72% and 94.75%.

1.INTRODUCTON

In digital systems for computing, data transmission, and network design, a multiplexer is an integral component of field-programmable gate arrays (FPGAs). Multiple data streams might share a single wire during a conversation [1]. Multiplexers are crucial to many field-programmable gate arrays (FPGAs) [2]. For the transmission and receiving of data by FPGAs, it is crucial. By reducing power and delay costs as much as possible, we aim to discover the best technical solution. There are several ways to build a multiplexer (e.g., PTL, CMOS, etc.), however a 2:1 Multiplexer may be achieved using just six transistors and a transmission gate. Figure 1 shows that the need for efficient digital circuits with reduced space requirements and low power consumption has increased due to the expansion of mobile applications. Battery life has surpassed other considerations for portable devices, such as size, speed, and price, since 1980 [5]. In recent decades, complementary metal-oxide semiconductor (CMOS) technology has been fundamental to the advancement of low-power device technology. Compared to previous low power methods, CMOS logic is superior due to its very low power consumption when working. Several nanoscale factors, including as latency, peak, equivalence, and strength, are investigated in this section [6-7].The essay's first section provides an overview of the topic, while the second section lays out the system's architecture in general.

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2.LITRATURE SURVEY

Because of the explosion of mobile devices, power dissipation has become an increasingly important issue in VLSI design. Because of the limitations of battery power, smaller and more energy-efficient circuits were created and used in portable devices. Potential byproducts of this innovation include a more compact battery and a lighter device [1]. Increasing the device's size (by adding a bigger battery) or redesigning the circuit to use less power is two ways to improve battery efficiency. While complementary metal-oxide semiconductor (CMOS) circuits have low static power requirements, they have significant dynamic power consumption. The CMOS circuit's power consumption has remained constant from 0 to c. While the pull-up network used half of the stored energy, the output load consumed all of it. The stored energy in the pull-down network is discharged into the ground via the load when the voltage hits zero. Power loss for a CMOS device after one cycle of operation is, hence, c [2]. One frequent data-path structure cell in CPU coprocessors is the multiplexer's square measure [3]. This kind of electrical circuit is often used whenever there is a requirement to merge two digital signals. Mix is short for time-division multiplexing, the technical name.

3. EXISITNG METHOD

With the emergence of mobile apps and other technical developments, power consumption has become a major concern in VLSI digital design [1-3]. Both low- and medium-performance portable devices and high-performance microprocessors have the same intrinsic limitation: power consumption. Clock speed and circuit density are constrained by the amount of power that can be employed in high-performance systems [4]. For the simple reason that it is not an easy task to both powers these circuits and disperses the heat they produce. Cell phones, biomedical devices, sensor networks, and other devices that rely on batteries to function have their power usage correlated with their battery life or charge duration. There will be changes to the device's size, weight, and cost. Static CMOS Logic has maintained its position as the design standard for the last 30 years, despite several attempts to provide more efficient and space-saving alternatives. There was earlier an improved option put forth, static complementary metal-oxide-semiconductor logic (PTL) [6-9].The PTL and static CMOS approaches were examined in a comprehensive comparison by Zimmermannetal. [7]. The XOR gates and multiplexers that are designed using pass-transistor logic (PTL) are ideal for use in arithmetic units because they are more efficient than the standard CMOS implementations [6, 8]. Implementations of logic gates like NANDs and NORs using PTL are slower and consume more power than their CMOS equivalents [8, 9]. This is because the output swings are reduced due to the threshold lowering across a single-channel pass transistor. Moreover, studies have shown [10] that PTLmonotonic gates leak much more than CMOS gates. Introducing the Gate Diffusion Input (GDI) technology in 2002 [11], we were able to reduce the power consumption and silicon footprint of VLSI digital circuits. Methods used to fabricate SOI and twin-well CMOS chips informed the GDI strategy. Several complicated logic operations may be executed.

Routes that save a lot of space. The GDI circuits exhibited reduced volatility compared to the PTL equivalents due to their lower thresholds. Power reductions were substantial because to the core GDI cell's enhanced logic flexibility and reduced transistor count, even if swing restoration circuits were still required. Using very modest GDI libraries, we have shown [11–14] that the GDI technique is highly efficient for both sequential logic and combinatorial implementations in very old CMOS processes. Combinatorial circuits, which include adders, multipliers, comparators, and counters, saw a 40% reduction in power usage when 0.18 nm and 0.8 nm technologies were used. More space and power efficiency were shown in GDIFlip-Flop (FF) implementations in the 0.35m and 0.18m processes compared to other reported Flip Flop approaches (DSTC, PowerPC, C2 MOS, HLFF) [14]. Since the GDImethod's introduction, several organizations have examined and used it [15–18]. Using a standard 0.18 m process, P.M. Lee et al. [15] examined the feasibility of FullGDIadders in 2007. Low voltage operation (below 0.5V) was investigated by F. Moradi et al. [16] utilizing GDI methods

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in 65nm technology with a complete adder implementation. According to the results of the trials, even a small subset of GDI's capabilities may improve the area, power, and power-delay goods. In this study, we take a look at the latest school of thought in GDI. The suggested GDI logic is more complicated, but it fits snugly into a typical CMOS process. We compare traditional CMOS logic to the enhanced GDI's properties in nanoscale technologies. We provide simulation results for basic GDI gates and corresponding CMOS gates while operating in the process and temperature corners of the 40nm low power CMOS technology. We demonstrate that GDI gates may cut active power consumption by 30% and leakage by 70% without compromising latency.

Table I: Boolean function synthesis through input configuration of a simple GDI cell

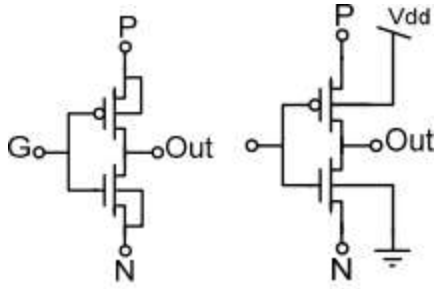
N	*P*	*G*	*Out*	*Function*
'0'	*B*	*A*	$\bar{A}B$	*F1*
B	*'1'*	*A*	$\bar{A}+B$	*F2*
'1'	*B*	*A*	$A+B$	*OR*
B	*'0'*	*A*	AB	*AND*
C	*B*	*A*	$\bar{A}B+AC$	*MUX*

A. SEDIT-Schematic Editor
B. TSPICE- Simulation program integrated circuit environment
C. WEDIT- wave form editor
1. PMOS :L=16nm W=64nm
2. NMOS L=16nm W=32nm
3. VDC=0.7V

Fig Basic GDI Cell

As seen in Figure 1(a), the basic cell was used in the initial GDI implementation. Although the basic cell is fundamentally different from CMOS inverters, it has certain surface-level similarities with them. The nMOS and pMOS share a gate input G, whereas the pMOS has a source/drain input P and the nMOS has a source/drain input R. The GDI cell makes use of these labels to distinguish between the different inputs. Another thing to keep in mind is that CMOS inverters aren't just sitting there doing nothing. Given that the bulks of nMOS and pMOS are linked to N and P, respectively, it is possible that they are dynamically skewed. In Table I, we can see how many different ways the basic GDI cell's input parameters may express Boolean operations. The GDI design

method uses only two transistors, as opposed to the six to twelve transistors used by Static CMOS and standard PTL



implementations for comparable operations.

IV.PROPSED METHOD

A potential decrease in transistor size is achievable with 16nm technology. Transistors' power consumption and latency are reduced as they are miniaturized, leading to a rise in the power delay product.

IV.I 2X1GDI MULTIPLIXER

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Fig6.12X1MultiplexerusingGDITechnology

There is a lot of overlap between CMOS logic and the TG technology's GDI method [5]. The CMOS logic's pull-up and pull-down networks use NMOS and PMOS transistors. Modern CMOS logic allows for the implementation of every logical operation imaginable. Despite CMOS's numerous benefits, including as dependability, small transistors, and improved performance at low speeds, the technology has two big drawbacks: slow speeds and high power consumption. An example of a common circuit design, the TG Gate (or Transmission Gate) makes use of a pair of PMOS and NMOS transistors connected in parallel. The drain terminal of the NMOS transistor is connected to the source terminal of the PMOS transistors. By fusing NMOS and PMOS, TG allows for a higher noise margin and fewer transistors to construct more sophisticated logic. Processing is sluggish, and there's a chance of a short circuit due to timing skew, which are two downsides. A new kind of cell known as a GDI (Gate Diffusion input) cell has been developed by scientists to circumvent this issue with CMOS [6]. The NMOS and PMOS transistors in GDI circuits are connected to the inputs, rather than the supply and ground, as they are in CMOS inverters. Figure 2 provides more clarification. Gate diffusion input (GDI) has been the focus of several studies that have examined its pros and cons. A gate-diffusion input multiplexer Right and Wrong We may say that the fact that the output isn't always close to Vdc is a downside, given that no system is perfect. However, there are a few advantages, like a minimum amount of transistors, minimal power consumption, and fast operation. Since NMOS produces a weak 1 when Sel=1 and B=1, the input B is sent to the output O.

Fig6.2 GADI technology simulation of a 2x1 multiplexer

The source terminals of the PMOS and NMOS devices are connected to signals A and B, respectively. Sel is connected to the MOS gates in Figure 4, and to the Mux's output in Figure 3, which regulates which inputs may reach the output. Figure 5 displays the output curve of the 1V power supply, which indicates a static power dissipation of 219.99pW.

PTBased multiplexer

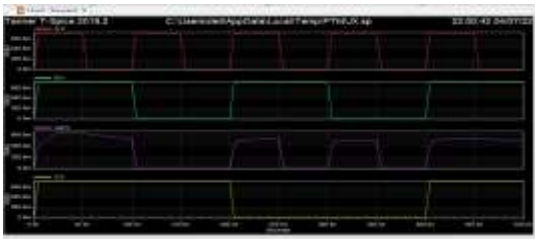

Fig6.3PT MultiplexerusingGDITechnology

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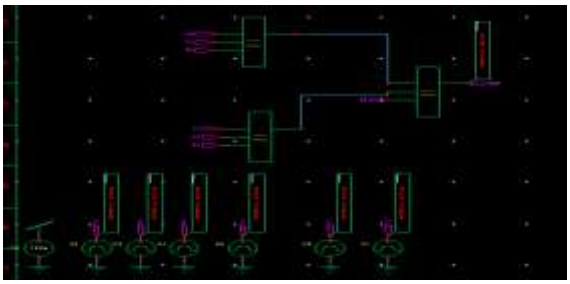


Fig6.4 SimulationofPTMultiplexerusingGDITechnology

A Cross-Interpreter Figure 3 is a schematic representation of the 2:1NMOSMUX, as per PT Research. Another method relies on CPL, or Complementary Pass Transistor Logic. Reducing the number of transistors required to build logic gates of different complexity is feasible by removing their superfluous counterparts [7]. Instead of using switches that are correctly linked to the power source, signals are transferred from the input node of the circuit to the output node using transistors. Although fewer active devices overall is a positive, the fact that output is not directly proportional to input is a negative. Figure 7 shows a mux architecture that uses pass transistors (PTs).Figures 8 and 9, which show the waveform and output plot, respectively, show the outcomes when the input is held static. An MSL, or single-level multiplexer with level restoration, is shown in Figure 10. The additional 2:1 MUX [8] will have a major effect on the whole region since PTL (Pass Transistor Logic) uses non-inverted and altered signals as its data sources. One such workaround might be to link the p-latch inverter to the complementary pass transistor (CPL) logic multiplexer's output terminal.

Fig6.5MSLMultiplexerusingGDITechnology

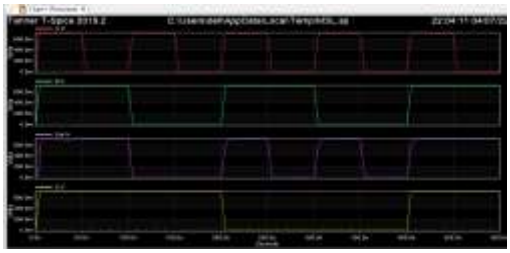
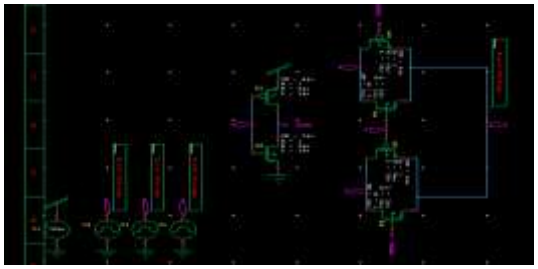


Fig6.6SimulationofMSLMultiplexerusingGDI Technology



The lack of a complement input is the primary benefit of MSL (Multiplexer single with level Restoration).2. User-Friendly the output is quite close to Vdc and zero in all three cases. Secondly, Downsides One disadvantage of this logic is the increased need for transistors. The second point is valid as a greater amount of energy is lost as heat instead of being used. This work successfully investigates and demonstrates a revolutionary 2:1 multiplier that is based on 90 nm technologies.

By contrasting latency and power, the optimal MUX may be identified. Research on power and delay has shown that different ones perform better and require less space while still minimizing energy loss, latency, transistor use, and total power consumption. The research shows that the pass transistor based mux, the multiplexer single with level

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restoration based mux, and the pass transistor based mux all have the best static power dissipation, latency, and overall performance.

PROPOSEDMETHOD

2:1Multiplexerusingtransmissiongate

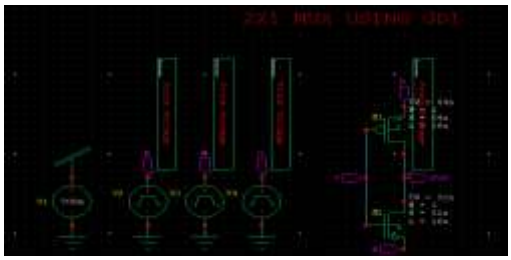

Fig6.72x1MultiplexerusingTGTechnology

Multipliers are fundamental to digital computing, routing, and communication systems like field-programmable gate arrays (FPGAs). A single transmission line may carry several bits of data [1]. Numerous multiplexers are essential to the operation of field-programmable gate arrays (FPGAs) [2]. It plays an essential role in FPGA signal routing. In particular, we want to find the technological node that has the highest probability of attaining the lowest conceivable average latency and power. While CMOS and PTL are two possible construction technologies for a 2:1 multiplexer, twelve transistors are required for transmission gate [3]. Figure 1 shows the rising rigidity of the power needs of portable applications, which is driving the demand for efficient digital circuits with low space and power consumption [4]. When it comes to mobile technology, battery life is now more important than speed, size, and price were in 1980 [5]. Complementary metal-oxide semiconductors, or CMOS, were the standard for electrical design that used little power for quite some time. Since CMOS uses far less power than other logic families, it outperforms previous low-power approaches. [6-7] the latency, average power, PDP, and EDP are some of the metrics that are tested in the nanoscale regime. The work is divided into four sections, the second of which is the i
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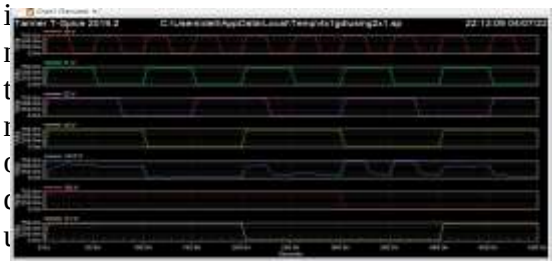

Fig6.8Simulationof2x1MultiplexerusingTG Technology

The 4:1 multiplexer is constructed using the 45 nm MOSFET model with TG-OR gates and the 32 nm model with TG-AND gates. An NMOS threshold voltage of 0.5088 volts and a PMOS threshold voltage of -0.450 volts characterize this 32 nm CMOS transistor. Both the PMOS and NMOS threshold voltages are -0.418V and 0.469, respectively, when the gate length is 45 nm. A model for predictive technology is used to get these figures [8]. Reducing power dissipation factors (PDP) is a primary goal for digital circuit designers when working with high frequencies and low power consumption. A characteristic of the PDP logic family is its power efficiency. Several factors have been investigated and contrasted in connection to the temperature and supply voltage, such as process variables, average power, power delay product, and energy delay

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product.

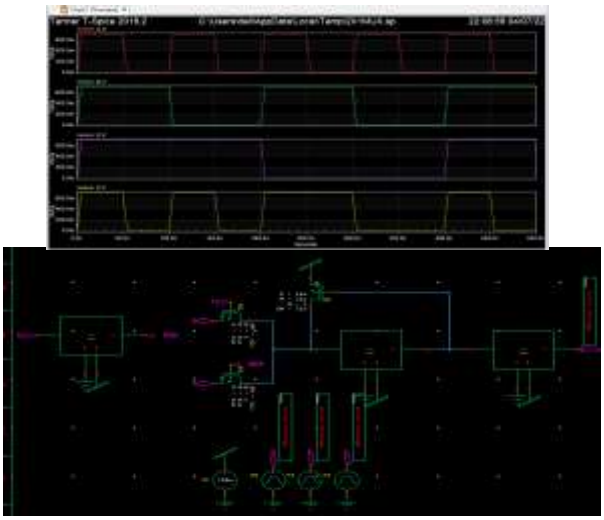

Fig6.9Schematicof4X1Using2x1MultiplexerusingTG Technology

Fig6.10Simulationof4X1Using2x1MultiplexerusingGDITechnology

On display in Figure 5 is a graph depicting the relationship between average power and supply voltage VDD.At 45 nanometers, the average power is lower than at 32 nanometers, according to the research. Power generation decreases when supply voltages drop. Because the supply voltage is reduced by 33% at 45 nm, the average power use drops from 90.82% at 32 nm to 84.75%. There is a plot of PDP vs. VDD (the supply voltage) in Figure 6. According to these findings, the 32-nanometer PDP is more compact than the 45-nanometer PDP. A lower input voltage results in a lower PDP. At 45 nanometers, the power delay product is 55.22%, down from 71.60% at 32 nanometers, when the supply voltage is reduced by 33%. Figure 7 shows the connection between EDP and VDD, the supply voltage. This study found that the 32-nanometer EDP is smaller than the 45-nanometer EDP. When the input voltage is dropped by 33%, the energy-delay product goes down from 32 nanometers to 32 nanometers and up from 16 nanometers to 31.5%.

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Power Results

VV1 from time 0 to 5e-07
Average power consumed -> 4.900000e-13 watts
Max power 4.900000e-13 at time 0
Min power 4.900000e-13 at time 0
```

Power analysis

COMPARISION TABLE

S.NO	METHODOLOGY	AVGP	MAXPower	MIN Power	AREA
1	Gate diffusion Input	1.995e-11	1.7927e-07	9.885e-13	2
2	Pass Transistor	2.0171e-08	9.6116e-07	5.7250e-09	4
3	MSL	5.3782e-06	1.1012e-05	9.4789e-07	9
4	TG(PROPOSED)	1.9792e-08	6.1358e-07	7.3633e-09	6

V.CONCLUSION

We tracked and analyzed many variables in connection to delay, PDP, and EDP, including supply voltage, temperature, and average power. Generally speaking, nodes with fewer technical skills have more energy usage. But in terms of speed, the less-advanced node is miles ahead of the more-advanced ones. When the supply voltage is cut in half, there is a corresponding rise of 209.56% in delay, 90.82% in average power, 71.60% in power delay product, and 12.12% in energy delay product at 16 nm. The power delay product has decreased by 55.24 percent and the energy delay product by 31.54 percent.

VI.FUTURESCOPE

Power and delay research shows that different ones are more efficient in different ways when it comes to space use, latency, energy consumption, transistor utilization, and performance. Based on the results, the best multiplexer and pass transistor are those that use MSL (Multiplexer single with level Restoration) and GDI (Gate

diffusion input), respectively, to achieve the lowest static power dissipation and average power dissipation, respectively. Memory, counters, LFSRs, and flip-flops may all be used to accomplish the suggested strategy.

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